H616 Datasheet

High Picture Quality 4K Decoding SoC

Revision 1.0

Dec.30, 2019

Revision History

Revision	Date	Description
1.0	Dec.30, 2019	Initial release version

Declaration

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, the interface timing, thermal and package, and part reliability of the H616 processor. For details about register descriptions of each module, see the ***Allwinner_H616_User_Manual***.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1. Overview

H616 is a high-performance SoC that supports 4K@60fps decoding for over-the-top(OTT) and Internet Protocol television(IPTV) markets. H616 integrates the 4-core 64-bit high performance Cortex™-A53 processor, built-in NEON acceleration engine, powerful CPU processing capabilities to meet a variety of differentiated business requirements. Maintain the best user experience in terms of stream compatibility, fluency of online video playback, image quality and performance of the whole machine. H616 supports multi formats of video decoder such as H.265, H.264, VP9, AVS2, AVS/AVS+, MPEG-1, MPEG-2, MPEG-4, VC1, VP8, and high-performance H.264 video encoder, which can meet the growing needs of multimedia playback, video communication. H616 also provides rich peripheral interfaces, such as USB2.0, SDIO3.0, 1000Mbps EMAC, TSC, SPI, UART, CIR, etc. H616 adopts the new generation of power consumption technology, and reduces power consumption of 20% than the last generation.

2. Features

2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 processor
- Power-efficient ARM v8 architecture
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced SIMD instruction for acceleration of media and signal processing functions
- Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit

2.2. GPU Architecture

- G31
- Supports OpenGL ES 1.0/2.0/3.2, Vulkan 1.1, OpenCL 2.0

2.3. Memory Subsystem

2.3.1. Boot ROM

- On-chip memory
- Supports system boot from the following devices:
  - SD/eMMC(SMHC0, SMHC2)
  - Nand Flash
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Supports mandatory upgrade process through SMHC0 and USB
- Secure brom supports load only certified firmware
- Secure brom ensures that the secure boot is a trusted environment

2.3.2. SDRAM

- 32-bit DDR4/DDR3/DDR3L/LPDDR3/LPDDR4 interface
- Memory capacity up to 4 GByte

2.3.3. NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 2 ready_busy signals
- Supports SLC/MLC/TLC flash and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

2.3.4. SMHC

- Three SD/MMC host controller (SMHC) interfaces
- SMHC0 controls the devices that comply with the Secure Digital (SD3.0)
  - 4-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output (SDIO3.0)
  - 4-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- SMHC2 controls the devices that comply with the Multimedia Card (eMMC 5.1)
  - 8-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.4. Video Engine

2.4.1. Video Decoding

- Supports video decoding up to 4K@60fps
- Supports multi-formats:
  - H.265 Main10@L5.1 up to 4K@60fps, or 6K@30fps
  - VP9 Profile 2 up to 4K@60fps
  - AVS2 JiZhun 10bit Profile up to 4K@60fps
  - H.264 BP/MP/HP@L4.2 up to 4K@30fps
  - H.263 BP up to 1080p@60fps
  - MPEG-4 SP/ASP@L5 up to 1080p@60fps
  - MPEG-2 MP/HL up to 1080p@60fps
  - MPEG-1 MP/HL up to 1080p@60fps
  - Xvid up to 1080p@60fps
  - Sorenson Spark up to 1080p@60fps
  - VP8 up to 1080p@60fps
  - AVS/AVS+ JiZhun Profile up to 1080p@60fps
  - WMV9/VC1 SP/MP/AP up to 1080p@60fps
  - JPEG HFIF file format up to 45MPPS

2.4.2. Video Encoding

- H.264 BP/MP/HP
- H.264 supports I/P frame, and only supports single reference frame
- MJPEG/JPEG baseline
- Maximum 16-megapixel(4096 x 4096) resolution for H.264 encoding
- H.264 encoding capability: 4K@25fps
- JPEG snapshot performance of 1080p@60fps independently
- Supports the constant bit rate(CBR)/variable bit rate(VBR) bit rate control mode, ranging from 256kbit/s to 100Mbit/s
- Encoding of eight regions of interest(ROIs)

2.5. Video and Graphics

2.5.1. Display Engine (DE)

- Output size up to 4096 x 2048
- Six configurable alpha blending channels
- Four overlay layers in each channel, and has an independent scaler
- Potter-duff compatible blending operation
- Supports AFBC buffer
- Supports keystone correction
- Input format: semi-planar YUV422/YUV420/YUV411/P010/P210 and planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports 10-bit processing path for HDR video
- Supports SDR/HDR10/Hybrid-log gamma EOTF and color space conversion
- Supports SmartColor™ 3.3 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement and fresh tone protection
  - Adaptive contrast enhancement
  - Adaptive de-noising for compression noise or mosquito noise with YUV420/YUV422 input
- Supports write back only for high efficient dual display and miracast
- Supports output format YUV444/YUV422/YUV420/RGB444 for 10/8bit
- Supports Register Configuration Queue for register update function

2.5.2. De-interlacer (DI)

- Supports off-line processing mode only
- Supports 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined input data format
- Supports 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined output data format for DIT, and YV12/planar YUV422 output data format for TNR
- Supports video resolution from 32 x 32 to 2048 x 1280 pixel
- Supports weave/pixel-motion-adaptive de-interlace method
- Supports temporal noise reduction function
- Supports film mode detection with video-on-film detection
- Performance: module clock 150 MHz for 1080p@60Hz

2.5.3. Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports input/output formats: YUV422(semi-planar and planar format)/YUV420(semi-planar and planar format)/P010/P210/P410/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ARGB2101010 and RGB565
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

2.6. System Peripherals

2.6.1. Timer

- The timer module implements the timing and counting functions, including Timer0, Timer1, Watchdog and AVS0, AVS1
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factors
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0

- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing
- 2 AVS counters (AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime
  - 12-bit frequency divider factor
  - Pause/Start function

2.6.2. High Speed Timer

- One high speed timer with 56-bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

2.6.3. RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Supports one solution without low-frequency crystal, a precise 32.768 kHz counter clock can be generated by using HOSC to calibrate the internal RC clock
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- 16 general purpose registers for storing power-off information

2.6.4. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 160 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization

2.6.5. DMA

- Up to 16-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.6.6. CCU

- 12 PLLs
- One on-chip RC oscillator and one external 24 MHz DCXO
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.6.7. Thermal Sensor Controller

- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Four thermal sensors: sensor0 located in the GPU, sensor1 located in the VE, sensor2 located in the CPU and sensor3 located in the DDR

2.6.8. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control and CP15 control
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc
- Including CPU debug control and status register

2.6.9. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE, DI, VE_R, VE, G2D parallel address mapping
- Supports DE, DI, VE_R, VE, G2D bypass function independently
- Supports DE, DI, VE_R, VE, G2D prefetch independently
- Supports DE, DI, VE_R, VE, G2D interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.7. Video Output

2.7.1. TVE

- Supports 1-ch TV CVBS output
- Supports NTSC and PAL mode
- Plug status auto detecting

2.7.2. HDMI

- Compatible with HDCP 2.2 and HDCP 1.4
- Supports DDC and SCDC
- Integrated CEC hardware engine
- Video support:
  - 2D Video: 4K/1080P/1080I/720P/576P/480P/576I/480I, up to 4K@60fps
  - 3D Video: 4K/1080P/720P/576P/480P, up to 4K@30fps
  - Supports RGB888/YUV444/YUV422 output
  - Color depth: 8/10-bit
  - HDR10: compliant with CTA-861.3 and SMPTE ST 2048
- Audio support:
  - Uncompressed audio formats: IEC60985 L-PCM audio samples, up to 192 kHz
  - Compressed audio formats: IEC61937 compressed audio, up to 1536 kHz

2.8. Audio Subsystem

2.8.1. Audio Codec

- Two audio digital-to-analog (DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95±2dB SNR@A-weight, -80±3dB THD+N, output Level more than 0.55Vrms
- One audio output
  - One differential LINEOUTP/N or single-ended LINEOUTL/R output
- Supports Dynamic Range Controller (DRC) adjusting the DAC playback
- One 128x24-bits FIFO for DAC data transmit
- Programmable FIFO thresholds
- DMA and Interrupt support

2.8.2. Audio HUB

- One Audio HUB
- Supports 2 Digital Audio MIXER(DAM)
- Supports 3 I2S/PCM interfaces for connecting external devices, and 1 I2S/PCM for connecting internal HDMI
- Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode
- I2S mode supports 8 channels, and 32-bit/192 kbit sample rate
- I2S and TDM modes support maximum 16 channels, and 32-bit/96 kbit sample rate

2.8.3. DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.8.4. OWA

- One OWA TX
- IEC-60958 transmitter functionality
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit, 20-bit and 24-bit data formats

2.9. Security Engine

2.9.1. Crypto Engine (CE)

- Supports Symmetrical algorithm: AES, DES, TDES, XTS
  - ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC mode for AES
  - 128/192/256-bit key for AES
  - 256-bit, 512-bit key for XTS
  - ECB, CBC, CTR, CBC-MAC mode for DES/TDES
- Supports Hash algorithm: MD5, SHA, HMAC
  - SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - HMAC-SHA1, HMAC-SHA256 for HMAC
  - MD5, SHA, HMAC are padded using hardware
- Supports Asymmetrical algorithm: RSA, ECC

  - RSA supports 512/1024/2048/4096-bit width
  - ECC supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG
- Supports 256-bit hardware TRNG
- Internal embedded DMA to do data transfer
- Supports secure and non-secure interfaces respectively
- Supports task chain mode for each request. Task or task chain are executed at request order
- 8 scatter group(sg) are supported for both input and output data
- DMA has multiple channels, each channel corresponds one suit of algorithm

2.9.2. Security ID

- Supports one EFUSE for chip ID and security application
- EFUSE has secure zone and non-secure zone

2.9.3. Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Set secure area of DRAM
- Set secure property that Master accesses to DRAM
- Set DRM area
- Set whether DRM master can access to DRM area or not

2.9.4. Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Set secure property of peripherals

2.10. External Peripherals

2.10.1. USB

- One USB 2.0 OTG(USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) in host mode
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
  - Up to 8 User-Configurable Endpoints (EPs) for Bulk, Isochronous and Interrupt bi-directional transfers
  - Supports (4KB+64Bytes) FIFO for all EPs (including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- Three USB 2.0 HOST(USB1, USB2, USB3), with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) device
  - Only USB2 supports USB standby

2.10.2. EMAC

- Two EMAC interfaces
  - EMAC0: 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces, for connecting the external EPHY
  - EMAC1: 10/100 Mbps Ethernet port with RMII interface, and it embedded with 100M EPHY
  - EMAC1 has no external pins

- EMAC0 and EMAC1 can use at the same time
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 KB TXFIFO for transmission packets and 16 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.10.3. UART

- Up to 6 UART controllers(UART0, UART1, UART2, UART3, UART4, UART5)
- UART0, UART5: 2-wire; UART1, UART2, UART3, UART4: 4-wire
- 2-wire UART can be used for printing; 4-wire UART can be used for flow control
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.10.4. SPI

- Up to 2 SPI controllers(SPI0, SPI1)
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
- Interrupt or DMA support
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1-bit to 32-bit
- Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI

2.10.5. Two Wire Interface (TWI)

- Up to 6 TWI controllers(TWI0, TWI1, TWI2, TWI3, TWI4, S_TWI0)
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master system supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in Master mode

2.10.6. CIR Receiver

- Full physical layer implementation
- Supports NEC format infrared data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.10.7. PWM

- 4 PWM channels(PWM1, PWM2, PWM3, PWM4)
- PWM23 pair consists of PWM2 and PWM3
- PWM23 pair supports deadzone function
- PWM1/4 has the single channel characteristics of PWM module, and has no pair function
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveforms: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0~24 MHz/100 MHz
- Various duty-cycle: 0%~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

2.10.8. Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit resolution
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Power supply voltage: 1.8 V, power reference voltage: 1.35 V, analog input and detected voltage range: 0~LEVELB (the maximum value is 1.266 V)

2.10.9. Transport Stream Controller (TSC)

- Supports SPI/SSI interface, interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Supports multiple transport stream packet (188, 192, 204) format
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

2.11. Package

- TFBGA284 balls, 0.65 mm ball pitch, 0.35 mm ball size, 14 mm x 12 mm body

3. Block Diagram

Figure 3-1 shows the system block diagram of the H616.

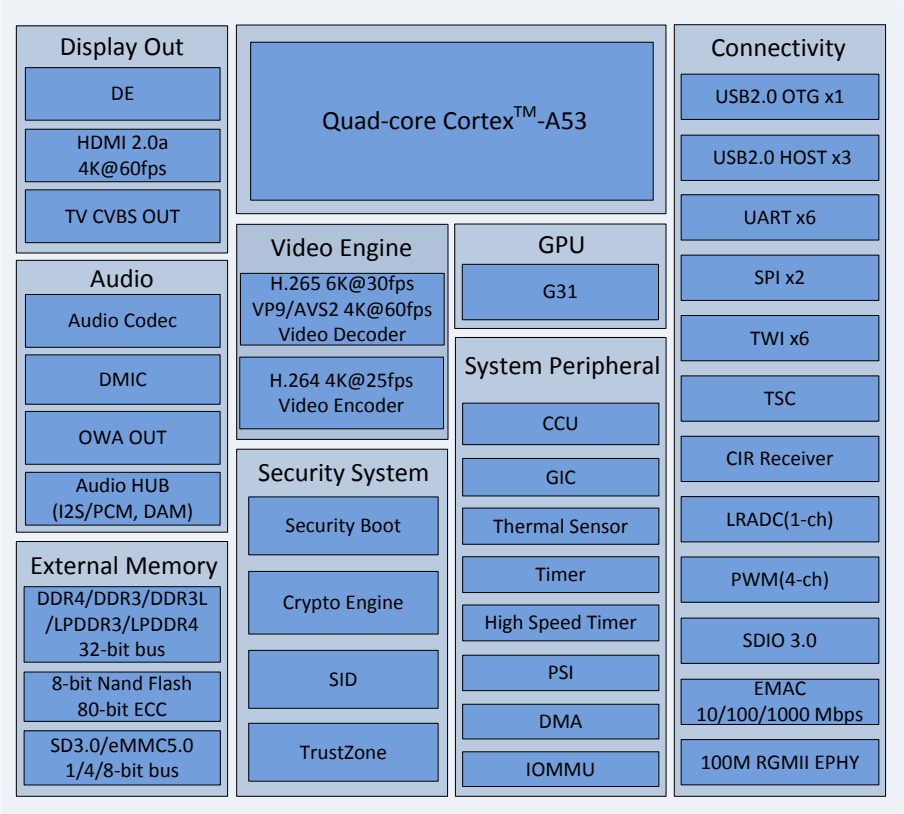


Figure 3-1. H616 System Block Diagram

Figure 3-2 shows the OTT Box solution of the H616.

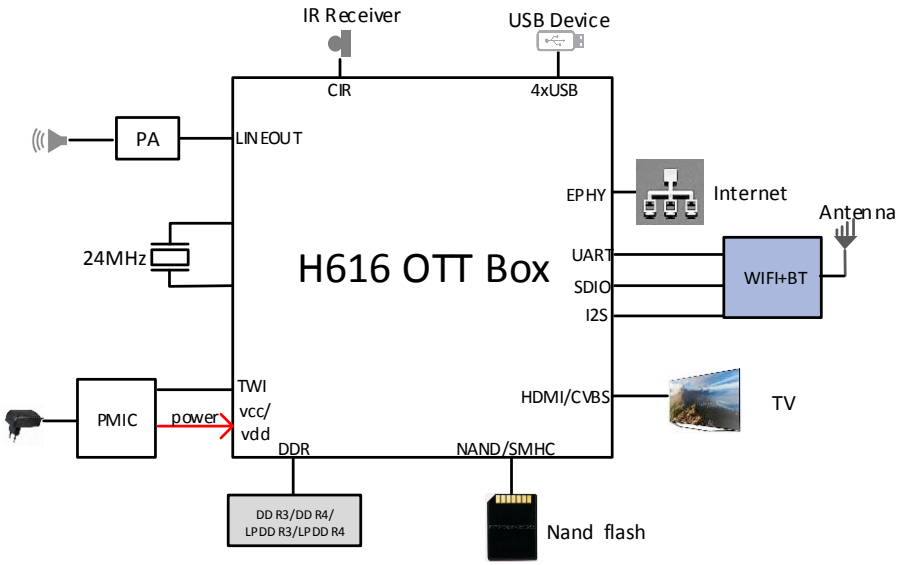


Figure 3-2. H616 OTT Box Solution

4. Pin Description

4.1. Pin Quantity

Table 4-1 lists the pin quantity of the H616.

Table 4-1. Pin Quantity

Pin Type	Quantity
I/O	191
Power	30
Ground	57
DDR Power	6
Total	284

4.2. Pin Characteristics

Table 4-2 lists the characteristics of the H616 pins from the following seven aspects.

[1].Ball#: Package ball numbers associated with each signals.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction

I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
P (Power),
G (Ground)

[4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled by software.

[6].Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.

[7].Power Supply: The voltage supply for the terminal's IO buffers.

Table 4-2. Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
SDRAM						
T21	SA0	O	Z	NA	NA	VCC_DRAM
U17	SA1	O	Z	NA	NA	VCC_DRAM
T18	SA2	O	Z	NA	NA	VCC_DRAM
T16	SA3	O	Z	NA	NA	VCC_DRAM
R18	SA4	O	Z	NA	NA	VCC_DRAM
P15	SA5	O	Z	NA	NA	VCC_DRAM
U20	SA6	O	Z	NA	NA	VCC_DRAM
N19	SA7	O	Z	NA	NA	VCC_DRAM
U19	SA8	O	Z	NA	NA	VCC_DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
N16	SA9	O	Z	NA	NA	VCC_DRAM
R19	SA10	O	Z	NA	NA	VCC_DRAM
U15	SA11	O	Z	NA	NA	VCC_DRAM
U16	SA12	O	Z	NA	NA	VCC_DRAM
P16	SA13	O	Z	NA	NA	VCC_DRAM
V20	SA14	O	Z	NA	NA	VCC_DRAM
N13	SA15	O	Z	NA	NA	VCC_DRAM
U18	SA16	O	Z	NA	NA	VCC_DRAM
N3	SDQ0	I/O	Z	NA	NA	VCC_DRAM
U4	SDQ1	I/O	Z	NA	NA	VCC_DRAM
N2	SDQ2	I/O	Z	NA	NA	VCC_DRAM
T4	SDQ3	I/O	Z	NA	NA	VCC_DRAM
U3	SDQ4	I/O	Z	NA	NA	VCC_DRAM
P1	SDQ5	I/O	Z	NA	NA	VCC_DRAM
T2	SDQ6	I/O	Z	NA	NA	VCC_DRAM
P2	SDQ7	I/O	Z	NA	NA	VCC_DRAM
P5	SDQ8	I/O	Z	NA	NA	VCC_DRAM
V3	SDQ9	I/O	Z	NA	NA	VCC_DRAM
P4	SDQ10	I/O	Z	NA	NA	VCC_DRAM
R4	SDQ11	I/O	Z	NA	NA	VCC_DRAM
R6	SDQ12	I/O	Z	NA	NA	VCC_DRAM
N4	SDQ13	I/O	Z	NA	NA	VCC_DRAM
P6	SDQ14	I/O	Z	NA	NA	VCC_DRAM
N5	SDQ15	I/O	Z	NA	NA	VCC_DRAM
T11	SDQ16	I/O	Z	NA	NA	VCC_DRAM
U12	SDQ17	I/O	Z	NA	NA	VCC_DRAM
T12	SDQ18	I/O	Z	NA	NA	VCC_DRAM
U9	SDQ19	I/O	Z	NA	NA	VCC_DRAM
T6	SDQ20	I/O	Z	NA	NA	VCC_DRAM
U5	SDQ21	I/O	Z	NA	NA	VCC_DRAM
T7	SDQ22	I/O	Z	NA	NA	VCC_DRAM
T5	SDQ23	I/O	Z	NA	NA	VCC_DRAM
R9	SDQ24	I/O	Z	NA	NA	VCC_DRAM
P7	SDQ25	I/O	Z	NA	NA	VCC_DRAM
N7	SDQ26	I/O	Z	NA	NA	VCC_DRAM
P9	SDQ27	I/O	Z	NA	NA	VCC_DRAM
P10	SDQ28	I/O	Z	NA	NA	VCC_DRAM
U11	SDQ29	I/O	Z	NA	NA	VCC_DRAM
P12	SDQ30	I/O	Z	NA	NA	VCC_DRAM
R12	SDQ31	I/O	Z	NA	NA	VCC_DRAM
U1	SDQM0	O	Z	NA	NA	VCC_DRAM
R3	SDQM1	O	Z	NA	NA	VCC_DRAM
T9	SDQM2	O	Z	NA	NA	VCC_DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
N10	SDQM3	O	Z	NA	NA	VCC_DRAM
R2	SDQS0P	I/O	Z	NA	NA	VCC_DRAM
U2	SDQS1P	I/O	Z	NA	NA	VCC_DRAM
V8	SDQS2P	I/O	Z	NA	NA	VCC_DRAM
V10	SDQS3P	I/O	Z	NA	NA	VCC_DRAM
R1	SDQS0N	I/O	Z	NA	NA	VCC_DRAM
V2	SDQS1N	I/O	Z	NA	NA	VCC_DRAM
U8	SDQS2N	I/O	Z	NA	NA	VCC_DRAM
U10	SDQS3N	I/O	Z	NA	NA	VCC_DRAM
P18	SACT	O	Z	NA	NA	VCC_DRAM
N21	SBA0	O	Z	NA	NA	VCC_DRAM
R15	SBA1	O	Z	NA	NA	VCC_DRAM
P20	SBG0	O	Z	NA	NA	VCC_DRAM
P21	SBG1	O	Z	NA	NA	VCC_DRAM
T14	SCKP	O	Z	NA	NA	VCC_DRAM
U14	SCKN	O	Z	NA	NA	VCC_DRAM
V15	SCKE0	O	Z	NA	NA	VCC_DRAM
P13	SCKE1	O	Z	NA	NA	VCC_DRAM
V17	SCS0	O	Z	NA	NA	VCC_DRAM
R20	SCS1	O	Z	NA	NA	VCC_DRAM
T20	SODT0	O	Z	NA	NA	VCC_DRAM
N20	SODT1	O	Z	NA	NA	VCC_DRAM
U21	SRST	O	Z	NA	NA	VCC_DRAM
L15	SZQ	AI	Z	NA	NA	VCC_DRAM
L9,L10,L11, L12,L13	VCC_DRAM	P	NA	NA	NA	NA
L14	VDD18_DRAM	P	NA	NA	NA	NA
GPIOC						
B1	PC0	I/O	Z	PU/PD	4	VCC_PC
C2	PC1	I/O	Z	PU/PD	4	VCC_PC
C1	PC2	I/O	Z	PU/PD	4	VCC_PC
D1	PC3	I/O	PU	PU/PD	4	VCC_PC
D2	PC4	I/O	PU	PU/PD	4	VCC_PC
D3	PC5	I/O	PU	PU/PD	4	VCC_PC
E2	PC6	I/O	PU	PU/PD	4	VCC_PC
F4	PC7	I/O	PU	PU/PD	4	VCC_PC
E3	PC8	I/O	Z	PU/PD	4	VCC_PC
F1	PC9	I/O	Z	PU/PD	4	VCC_PC
F2	PC10	I/O	Z	PU/PD	4	VCC_PC
F3	PC11	I/O	Z	PU/PD	4	VCC_PC
G2	PC12	I/O	Z	PU/PD	4	VCC_PC
G3	PC13	I/O	Z	PU/PD	4	VCC_PC
H1	PC14	I/O	Z	PU/PD	4	VCC_PC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
H2	PC15	I/O	Z	PU/PD	4	VCC_PC
H3	PC16	I/O	Z	PU/PD	4	VCC_PC
F5	VCC_PC	P	NA	NA	NA	NA
GPIOF						
J2	PF0	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
J3	PF1	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
K1	PF2	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
K3	PF3	I/O	PU	PU/PD	4	VCC_IO, or VCC_PLL
L2	PF4	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
L3	PF5	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
K2	PF6	I/O	PU	PU/PD	4	VCC_IO, or VCC_PLL
GPIOG						
A6	PG0	I/O	Z	PU/PD	4	VCC_PG
C7	PG1	I/O	PU	PU/PD	4	VCC_PG
C6	PG2	I/O	PU	PU/PD	4	VCC_PG
B5	PG3	I/O	PU	PU/PD	4	VCC_PG
C5	PG4	I/O	PU	PU/PD	4	VCC_PG
B7	PG5	I/O	PU	PU/PD	4	VCC_PG
A4	PG6	I/O	Z	PU/PD	4	VCC_PG
B4	PG7	I/O	Z	PU/PD	4	VCC_PG
C4	PG8	I/O	Z	PU/PD	4	VCC_PG
B3	PG9	I/O	Z	PU/PD	4	VCC_PG
C8	PG10	I/O	Z	PU/PD	4	VCC_PG
B10	PG11	I/O	Z	PU/PD	4	VCC_PG
C9	PG12	I/O	Z	PU/PD	4	VCC_PG
C10	PG13	I/O	Z	PU/PD	4	VCC_PG
B9	PG14	I/O	Z	PU/PD	4	VCC_PG
A8	PG15	I/O	Z	PU/PD	4	VCC_PG
B8	PG16	I/O	Z	PU/PD	4	VCC_PG
C3	PG17	I/O	Z	PU/PD	4	VCC_PG
A2	PG18	I/O	Z	PU/PD	4	VCC_PG
B2	PG19	I/O	Z	PU/PD	4	VCC_PG
D7	VCC_PG	P	NA	NA	NA	NA
GPIOH						
D16	PH0	I/O	Z	PU/PD	4	VCC_IO
D15	PH1	I/O	Z	PU/PD	4	VCC_IO
B15	PH2	I/O	Z	PU/PD	4	VCC_IO
C15	PH3	I/O	Z	PU/PD	4	VCC_IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
A14	PH4	I/O	Z	PU/PD	4	VCC_IO
B14	PH5	I/O	Z	PU/PD	4	VCC_IO
C14	PH6	I/O	Z	PU/PD	4	VCC_IO
B12	PH7	I/O	Z	PU/PD	4	VCC_IO
C13	PH8	I/O	Z	PU/PD	4	VCC_IO
A12	PH9	I/O	Z	PU/PD	4	VCC_IO
B13	PH10	I/O	Z	PU/PD	4	VCC_IO
GPIOI						
H6	PI0	I/O	Z	PU/PD	4	VCC_PI
D4	PI1	I/O	Z	PU/PD	4	VCC_PI
G6	PI2	I/O	Z	PU/PD	4	VCC_PI
E4	PI3	I/O	Z	PU/PD	4	VCC_PI
G5	PI4	I/O	Z	PU/PD	4	VCC_PI
H4	PI5	I/O	Z	PU/PD	4	VCC_PI
H5	PI6	I/O	Z	PU/PD	4	VCC_PI
G4	PI7	I/O	Z	PU/PD	4	VCC_PI
E6	PI8	I/O	Z	PU/PD	4	VCC_PI
D5	PI9	I/O	Z	PU/PD	4	VCC_PI
L5	PI10	I/O	Z	PU/PD	4	VCC_PI
K4	PI11	I/O	Z	PU/PD	4	VCC_PI
K5	PI12	I/O	Z	PU/PD	4	VCC_PI
E5	PI13	I/O	Z	PU/PD	4	VCC_PI
L6	PI14	I/O	Z	PU/PD	4	VCC_PI
L4	PI15	I/O	Z	PU/PD	4	VCC_PI
K6	PI16	I/O	Z	PU/PD	4	VCC_PI
J6	VCC_PI	P	NA	NA	NA	NA
GPIOL						
C18	PL0	I/O	PU	PU/PD	4	VCC_PLL
B18	PL1	I/O	PU	PU/PD	4	VCC_PLL
System						
B17	FEL	I	PU	PU/PD	NA	VCC_IO
C16	JTAG_SEL	I	PU	PU/PD	NA	VCC_IO
A16	RESET	I/O	No Pull	PU/PD	NA	VCC_PLL
D14	PLLTEST	AO	NA	NA	NA	VCC_PLL
LRADC						
L18	LRADC	AI	NA	NA	NA	AVCC
USB						
J19	USB0_DM	AI/O	NA	NA	NA	VCC_USB
J20	USB0_DP	AI/O	NA	NA	NA	VCC_USB
M19	USB1_DM	AI/O	NA	NA	NA	VCC_USB
M20	USB1_DP	AI/O	NA	NA	NA	VCC_USB
K19	USB2_DM	AI/O	NA	NA	NA	VCC_USB
K20	USB2_DP	AI/O	NA	NA	NA	VCC_USB

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
L19	USB3_DM	AI/O	NA	NA	NA	VCC_USB
L20	USB3_DP	AI/O	NA	NA	NA	VCC_USB
M18	VCC_USB	P	NA	NA	NA	NA
HDMI						
E20	HTX0N	AO	NA	NA	NA	VCC_HDMI
E19	HTX0P	AO	NA	NA	NA	VCC_HDMI
D21	HTX1N	AO	NA	NA	NA	VCC_HDMI
D20	HTX1P	AO	NA	NA	NA	VCC_HDMI
C20	HTX2N	AO	NA	NA	NA	VCC_HDMI
C19	HTX2P	AO	NA	NA	NA	VCC_HDMI
F21	HTXCN	AO	NA	NA	NA	VCC_HDMI
F20	HTXCP	AO	NA	NA	NA	VCC_HDMI
G17	HCEC	I/O	NA	NA	NA	VCC_HDMI
G18	HHPD	I/O	NA	NA	NA	VCC_HDMI
F19	HSCL	O	NA	NA	NA	VCC_HDMI
G21	HSDA	I/O	NA	NA	NA	VCC_HDMI
F18	VCC_HDMI	P	NA	NA	NA	NA
TV OUT						
J21	TV_OUT	AO	NA	NA	NA	VCC_TV
H20	VCC_TV	P	NA	NA	NA	NA
Audio Codec						
J18	VRA1	AO	NA	NA	NA	AVCC
J17	VRA2	AO	NA	NA	NA	AVCC
H17	AVCC	P	NA	NA	NA	NA
G19	LINEOUTL	AO	NA	NA	NA	AVCC
G20	LINEOUTR	AO	NA	NA	NA	AVCC
H18	AGND	G	NA	NA	NA	NA
K18	REXT	AO	NA	NA	NA	AVCC
AC+EPHY						
D17	AC_VRA1	AO	NA	NA	NA	AC_AVCC
D18	AC_AVCC	P	NA	NA	NA	NA
B19	EPHY_RTX	AI	NA	NA	NA	VCC_EPHY
B21	EPHY_RXN	AI/O	NA	NA	NA	VCC_EPHY
B20	EPHY_RXP	AI/O	NA	NA	NA	VCC_EPHY
A20	EPHY_TXN	AI/O	NA	NA	NA	VCC_EPHY
A19	EPHY_TXP	AI/O	NA	NA	NA	VCC_EPHY
E18	VCC_EPHY	P	NA	NA	NA	NA
DCXO						
B11	DXIN	AI	NA	NA	NA	VCC_DCXO
C12	DXOUT	AO	NA	NA	NA	VCC_DCXO
D13	DXLDO_OUT	AO	NA	NA	NA	VCC_DCXO
C11	REFCLK_OUT	AO	NA	NA	NA	VCC_DCXO
D11	VCC_DCXO	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
Power						
D10	VCC_IO	P	NA	NA	NA	NA
H8,H9,J8,J9, J10,J11	VDD_CPU	P	NA	NA	NA	NA
L8	VDD_CPUFB	P	NA	NA	NA	NA
F9,F10,G8,G9	VDD_GPU	P	NA	NA	NA	NA
F8	VDD_GPUFB	P	NA	NA	NA	NA
F11,F12,G10, G11,G12,F13	VDD_SYS	P	NA	NA	NA	NA
D12	VCC_PLL	P	NA	NA	NA	NA
Ground						
A1,A10,A18, A21,B16,B6, D19,F14,F15, G13,G14,G15, H10,H11,H12, H13,H14,H15, H19,J12,J13, J14,J15,K10, K11,K12,K13, K14,K15,K8, K9,L21,M1, M2,M3,N12, N15,N18,N6, N9,P3,R21, R5,T1,T10, T15,T17,T3, T8,U13,U6, V1,V12,V19, V21,V5	GND	G	NA	NA	NA	NA

4.3. GPIO Multiplex Function

The following table provides a description of the H616 GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function.

Table 4-3. GPIO Multiplex Function

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PC0	GPIOC	I/O	NAND_WE	SDC2_DS	SPI0_CLK		PC_EINT0
PC1		I/O	NAND_ALE	SDC2_RST			PC_EINT1
PC2		I/O	NAND_CLE		SPI0_MOSI		PC_EINT2
PC3		I/O	NAND_CE1		SPI0_CS0	BOOT_SEL1	PC_EINT3
PC4		I/O	NAND_CE0		SPI0_MISO	BOOT_SEL2	PC_EINT4
PC5		I/O	NAND_RE	SDC2_CLK		BOOT_SEL3	PC_EINT5
PC6		I/O	NAND_RB0	SDC2_CMD		BOOT_SEL4	PC_EINT6
PC7		I/O	NAND_RB1		SPI0_CS1		PC_EINT7
PC8		I/O	NAND_DQ7	SDC2_D3			PC_EINT8

PC9		I/O	NAND_DQ6	SDC2_D4			PC_EINT9
PC10		I/O	NAND_DQ5	SDC2_D0			PC_EINT10
PC11		I/O	NAND_DQ4	SDC2_D5			PC_EINT11
PC12		I/O	NAND_DQS				PC_EINT12
PC13		I/O	NAND_DQ3	SDC2_D1			PC_EINT13
PC14		I/O	NAND_DQ2	SDC2_D6			PC_EINT14
PC15		I/O	NAND_DQ1	SDC2_D2	SPI0_WP		PC_EINT15
PC16		I/O	NAND_DQ0	SDC2_D7	SPI0_HOLD		PC_EINT16
PF0	GPIOF	I/O	SDC0_D1	JTAG_MS			PF_EINT0
PF1		I/O	SDC0_D0	JTAG_DI			PF_EINT1
PF2		I/O	SDC0_CLK	UART0_TX			PF_EINT2
PF3		I/O	SDC0_CMD	JTAG_DO			PF_EINT3
PF4		I/O	SDC0_D3	UART0_RX			PF_EINT4
PF5		I/O	SDC0_D2	JTAG_CK			PF_EINT5
PF6		I/O					PF_EINT6
PG0	GPIOG	I/O	SDC1_CLK				PG_EINT0
PG1		I/O	SDC1_CMD				PG_EINT1
PG2		I/O	SDC1_D0				PG_EINT2
PG3		I/O	SDC1_D1				PG_EINT3
PG4		I/O	SDC1_D2				PG_EINT4
PG5		I/O	SDC1_D3				PG_EINT5
PG6		I/O	UART1_TX		JTAG_MS		PG_EINT6
PG7		I/O	UART1_RX		JTAG_CK		PG_EINT7
PG8		I/O	UART1_RTS	PLL_LOCK_DBG	JTAG_DO		PG_EINT8
PG9		I/O	UART1_CTS		JTAG_DI		PG_EINT9
PG10		I/O	H_I2S2_MCLK	X32KFOUT			PG_EINT10
PG11		I/O	H_I2S2_BCLK		BIST_RESULT0		PG_EINT11
PG12		I/O	H_I2S2_LRCK		BIST_RESULT1		PG_EINT12
PG13		I/O	H_I2S2_DOUT0	H_I2S2_DIN1	BIST_RESULT2		PG_EINT13
PG14		I/O	H_I2S2_DIN0	H_I2S2_DOUT1	BIST_RESULT3		PG_EINT14
PG15		I/O	UART2_TX			TWI4_SCK	PG_EINT15
PG16		I/O	UART2_RX			TWI4_SDA	PG_EINT16
PG17		I/O	UART2_RTS			TWI3_SCK	PG_EINT17
PG18		I/O	UART2_CTS			TWI3_SDA	PG_EINT18
PG19		I/O			PWM1		PG_EINT19
PH0	GPIOH	I/O	UART0_TX		PWM3	TWI1_SCK	PH_EINT0
PH1		I/O	UART0_RX		PWM4	TWI1_SDA	PH_EINT1
PH2		I/O	UART5_TX	OWA_MCLK	PWM2	TWI2_SCK	PH_EINT2
PH3		I/O	UART5_RX		PWM1	TWI2_SDA	PH_EINT3
PH4		I/O		OWA_OUT		TWI3_SCK	PH_EINT4
PH5		I/O	UART2_TX	H_I2S3_MCLK	SPI1_CS0	TWI3_SDA	PH_EINT5
PH6		I/O	UART2_RX	H_I2S3_BCLK	SPI1_CLK	TWI4_SCK	PH_EINT6
PH7		I/O	UART2_RTS	H_I2S3_LRCK	SPI1_MOSI	TWI4_SDA	PH_EINT7
PH8		I/O	UART2_CTS	H_I2S3_DOUT0	SPI1_MISO	H_I2S3_DIN1	PH_EINT8
PH9		I/O		H_I2S3_DIN0	SPI1_CS1	H_I2S3_DOUT1	PH_EINT9
PH10		I/O		IR_RX	TCON_TRIG1		PH_EINT10
PI0	GPIOI	I/O	RGMII_RXD3/ RMII_NULL	DMIC_CLK	H_I2S0_MCLK	HDMI_SCL	PI_EINT0
PI1		I/O	RGMII_RXD2/ RMII_NULL	DMIC_DATA0	H_I2S0_BCLK	HDMI_SDA	PI_EINT1
PI2		I/O	RGMII_RXD1/ RMII_RXD1	DMIC_DATA1	H_I2S0_LRCK	HDMI_CEC	PI_EINT2
PI3		I/O	RGMII_RXD0/ RMII_RXD0	DMIC_DATA2	H_I2S0_DOUT0	H_I2S0_DIN1	PI_EINT3
PI4		I/O	RGMII_RXCK/	DMIC_DATA3	H_I2S0_DIN0	H_I2S0_DOUT1	PI_EINT4

			RMII_NULL				
PI5		I/O	RGMII_RXCTL/ RMII_CRS_DV	UART2_TX	TS0_CLK	TWI0_SCK	PI_EINT5
PI6		I/O	RGMII_NULL/ RMII_RXER	UART2_RX	TS0_ERR	TWI0_SDA	PI_EINT6
PI7		I/O	RGMII_TXD3/ RMII_NULL	UART2_RTS	TS0_SYNC	TWI1_SCK	PI_EINT7
PI8		I/O	RGMII_TXD2/ RMII_NULL	UART2_CTS	TS0_DVLD	TWI1_SDA	PI_EINT8
PI9		I/O	RGMII_TXD1/ RMII_TXD1	UART3_TX	TS0_D0	TWI2_SCK	PI_EINT9
PI10		I/O	RGMII_TXD0/ RMII_TXD0	UART3_RX	TS0_D1	TWI2_SDA	PI_EINT10
PI11		I/O	RGMII_TXCK/ RMII_TXCK	UART3_RTS	TS0_D2	PWM1	PI_EINT11
PI12		I/O	RGMII_TXCTL/ RMII_TXEN	UART3_CTS	TS0_D3	PWM2	PI_EINT12
PI13		I/O	RGMII_CLKIN/ RMII_NULL	UART4_TX	TS0_D4	PWM3	PI_EINT13
PI14		I/O	MDC	UART4_RX	TS0_D5	PWM4	PI_EINT14
PI15		I/O	MDIO	UART4_RTS	TS0_D6	CLK_FANOUT0	PI_EINT15
PI16		I/O	EPHY_25M	UART4_CTS	TS0_D7	CLK_FANOUT1	PI_EINT16
PL0	GPIOL	I/O		S_TWI0_SCK			
PL1		I/O		S_TWI0_SDA			

4.4. Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.

[1].Signal Name: The name of every signal.

[2].Description: The detailed function description of every signal.

[3].Type: Denotes the signal direction:

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-4. Detailed Signal Description

Signal Name[1]	Description[2]	Type[3]
DRAM		
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQS[3:0]P	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O
SDQS[3:0]N	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	O
SCKP	DRAM Active-High Clock Signal to the Memory Device	O
SCKN	DRAM Active-Low Clock Signal to the Memory Device	O

Signal Name[1]	Description[2]	Type[3]
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device	O
SA[16:0]	DRAM Address Signal to the Memory Device	O
SBA[1:0]	DRAM Bank Address Signal to the Memory Device	O
SBG[1:0]	DRAM Bank Group Address Signal to the Memory Device	O
SACT	DRAM Activation Command Output	O
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SODT[1:0]	DRAM On-Die Termination Output Signal	O
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
SRST	DRAM Reset Signal to the Memory Device	O
VCC_DRAM	DRAM Power Supply	P
VDD18_DRAM	SDRAM Controller Power Supply	P
System Control		
FEL	Boot Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process. For more details, see section 3.4 “BROM System” in the ***Allwinner H616 User Manual***.	I
BOOT_SEL[4:1]	Boot Media Select	I
JTAG_SEL	JTAG Mode Select The signal is used to select the port from which JTAG function outputs.	I
PLLTEST	PLL Test Signal	OD
RESET	Reset Signal(low active)	I/O
X32KFOUT	32.768kHz Clock Fanout(provide low frequency clock to the external device)	OD
DCXO		
DXLDO_OUT	Internal Supply Regulator Output	AO
REFCLK_OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
VCC_DCXO	Digital Compensated Crystal Oscillator Power Supply	P
USB		
USB0_DM	USB0 Data Signal DM	AI/O
USB0_DP	USB0 Data Signal DP	AI/O
USB1_DM	USB1 Data Signal DM	AI/O
USB1_DP	USB1 Data Signal DP	AI/O
USB2_DM	USB2 Data Signal DM	AI/O
USB2_DP	USB2 Data Signal DP	AI/O
USB3_DM	USB3 Data Signal DM	AI/O
USB3_DP	USB3 Data Signal DP	AI/O
VCC_USB	USB Power Supply	P
LRADC		
LRADC	Low Rate ADC Input Channel	AI
AUDIO CODEC Analog Part		
LINEOUTL	Stereo Lineout Output Left Channel	AO

Signal Name[1]	Description[2]	Type[3]
LINEOUTR	Stereo Lineout Output Right Channel	AO
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
REXT	External Reference Pin	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
HDMI		
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HCEC	HDMI Consumer Electronics Control	I/O
HHPD	HDMI Hot Plug Detection Signal	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
VCC_HDMI	HDMI Power Supply	P
TVOUT		
TV_OUT	TV-out Output	AO
VCC_TV	TV-out Power Supply	P
AC+EPHY		
AC_VRA1	Audio Codec Reference Voltage	AO
AC_AVCC	Audio Codec Power Supply	P
EPHY_RTX	EPHY External Resistance to Ground	AI
EPHY_RXN	EPHY Transceiver Negative Output/Input	AI/O
EPHY_RXP	EPHY Transceiver Positive Output/Input	AI/O
EPHY_TXN	EPHY Transceiver Negative Output/Input	AI/O
EPHY_TXP	EPHY Transceiver Positive Output/Input	AI/O
VCC_EPHY	EPHY Power Supply	P
NAND Flash		
NAND_WE	Nand Flash Write Enable	O
NAND_ALE	Nand Flash Address Latch Enable	O
NAND_CLE	Nand Flash Command Latch Enable	O
NAND_CE[1:0]	Nand Flash Chip Select	O
NAND_RE	Nand Flash Read Enable	O
NAND_RB[1:0]	Nand Flash Ready/Busy Status Indicator Signal	I
NAND_DQ[7:0]	Nand Flash Data Bit	I/O
NAND_DQS	Nand Flash Data Strobe	I/O
SMHC		
SDC0_D[3:0]	SDC0 Data Bit	I/O
SDC0_CLK	SDC0 Clock	O

Signal Name[1]	Description[2]	Type[3]
SDC0_CMD	SDC0 Command Signal	I/O,OD
SDC1_D[3:0]	SDC1 Data Bit	I/O
SDC1_CLK	SDC1 Clock	O
SDC1_CMD	SDC1 Command Signal	I/O,OD
SDC2_D[7:0]	SDC2 Data Bit	I/O
SDC2_CLK	SDC2 Clock	O
SDC2_CMD	SDC2 Command Signal	I/O,OD
SDC2_DS	SDC2 Data Strobe	I
SDC2_RST	SDC2 Reset	O
Audio HUB		
H_I2S0_MCLK	I2S0 Master Clock	O
H_I2S0_LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
H_I2S0_BCLK	I2S0/PCM0 Sample Rate Clock	I/O
H_I2S0_DOUT[1:0]	I2S0/PCM0 Serial Data Output Channel [1:0]	O
H_I2S0_DIN[1:0]	I2S0/PCM0 Serial Data Input Channel [1:0]	I
H_I2S2_MCLK	I2S2 Master Clock	O
H_I2S2_LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
H_I2S2_BCLK	I2S2/PCM2 Sample Rate Clock	I/O
H_I2S2_DOUT[1:0]	I2S2/PCM2 Serial Data Output Channel [1:0]	O
H_I2S2_DIN[1:0]	I2S2/PCM2 Serial Data Input Channel [1:0]	I
H_I2S3_MCLK	I2S3 Master Clock	O
H_I2S3_LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
H_I2S3_BCLK	I2S3/PCM3 Sample Rate Clock	I/O
H_I2S3_DOUT[1:0]	I2S3/PCM3 Serial Data Output Channel [1:0]	O
H_I2S3_DIN[1:0]	I2S3/PCM3 Serial Data Input Channel [1:0]	I
DMIC		
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA[3:0]	Digital Microphone Data Input	I
OWA		
OWA_OUT	One Wire Audio Output	O
OWA_MCLK	One Wire Audio Master Clock	O
Interrupt		
PC_EINT[16:0]	GPIO C Interrupt	I
PF_EINT[6:0]	GPIO F Interrupt	I
PG_EINT[19:0]	GPIO G Interrupt	I
PH_EINT[10:0]	GPIO H Interrupt	I
PI_EINT[16:0]	GPIO I Interrupt	I
PWM		
PWM[4:1]	Pulse Width Modulation Output Channel [4:1]	I/O
CIR Receiver		
IR_RX	Consumer Infrared Receiver	I
EMAC		
RGMII_RXD3/RMII_NULL	RGMII Receive Data3	I
RGMII_RXD2/RMII_NULL	RGMII Receive Data2	I

Signal Name[1]	Description[2]	Type[3]
RGMII_RXD1/RMII_RXD1	RGMII/RMII Receive Data1	I
RGMII_RXD0/RMII_RXD0	RGMII/RMII Receive Data0	I
RGMII_RXCK/RMII_NULL	RGMII Receive Clock	I
RGMII_RXCTL/RMII_CRS_DV	RGMII Receive Control/RMII Carrier Sense Receive Data Valid	I
RGMII_NULL/RMII_RXER	RMII Receive Error	I
RGMII_TXD3/RMII_NULL	RGMII Transmit Data3	O
RGMII_TXD2/RMII_NULL	RGMII Transmit Data2	O
RGMII_TXD1/RMII_TXD1	RGMII/RMII Transmit Data1	O
RGMII_TXD0/RMII_TXD0	RGMII/RMII Transmit Data0	O
RGMII_TXCK/RMII_TXCK	RGMII/RMII Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII_TXCTL/RMII_TXEN	RGMII Transmit Control/RMII Transmit Enable	O
RGMII_CLKIN/RMII_NULL	RGMII Transmit Clock from External	I
MDC	RGMII/RMII Management Data Clock	O
MDIO	RGMII/RMII Management Data Input/Output	I/O
EPHY_25M	25MHz Output for EPHY	O
TSC		
TS0_CLK	Transport Stream Clock	I
TS0_ERR	Transport Stream Error Indicate	I
TS0_SYNC	Transport Stream Sync	I
TS0_DVLD	Transport Stream Data Valid	I
TS0_D[7:0]	Transport Stream Data	I
SPI		
SPI0_CS0	SPI0 Chip Select0 Signal, Low Active	I/O
SPI0_CS1	SPI0 Chip Select1 Signal, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0_WP	SPI0 Write Protect, Low Active	I/O
SPI0_HOLD	SPI0 Hold Signal	I/O
SPI1_CS0	SPI1 Chip Select0 Signal, Low Active	I/O
SPI1_CS1	SPI1 Chip Select1 Signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear to Send	I
UART1_RTS	UART1 Data Request to Send	O
UART2_TX	UART2 Data Transmit	O

Signal Name[1]	Description[2]	Type[3]
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear to Send	I
UART2_RTS	UART2 Data Request to Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear to Send	I
UART3_RTS	UART3 Data Request to Send	O
UART4_TX	UART4 Data Transmit	O
UART4_RX	UART4 Data Receive	I
UART4_CTS	UART4 Data Clear to Send	I
UART4_RTS	UART4 Data Request to Send	O
UART5_TX	UART5 Data Transmit	O
UART5_RX	UART5 Data Receive	I
TWI		
TWI0_SCK	TWI0 Serial Clock Signal	I/O
TWI0_SDA	TWI0 Serial Data Signal	I/O
TWI1_SCK	TWI1 Serial Clock Signal	I/O
TWI1_SDA	TWI1 Serial Data Signal	I/O
TWI2_SCK	TWI2 Serial Clock Signal	I/O
TWI2_SDA	TWI2 Serial Data Signal	I/O
TWI3_SCK	TWI3 Serial Clock Signal	I/O
TWI3_SDA	TWI3 Serial Data Signal	I/O
TWI4_SCK	TWI4 Serial Clock Signal	I/O
TWI4_SDA	TWI4 Serial Data Signal	I/O
S_TWI0_SCK	S_TWI0 Serial Clock Signal	I/O
S_TWI0_SDA	S_TWI0 Serial Data Signal	I/O
JTAG		
JTAG_MS	JTAG Mode Select	I
JTAG_CK	JTAG Clock Signal	I
JTAG_DO	JTAG Data Output	O
JTAG_DI	JTAG Data Input	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
AVCC	Analog Part Power		-0.3	2.16	V
AC_AVCC	AC Chip Analog Part Power		-0.3	2.16	V
VCC_PC	Digital GPIO C Power		-0.3	3.96	V
VCC_PG	Digital GPIO G Power		-0.3	3.96	V
VCC_PI	Digital GPIO I Power		-0.3	3.96	V
VCC_IO	GPIO F, GPIO H and System Control Power		-0.3	3.96	V
VCC_USB	USB Analog Power		-0.3	3.96	V
VCC_HDMI	HDMI Power		-0.3	2.16	V
VCC_TV	TV OUT Power		-0.3	2.16	V
VCC_DCXO	DCXO Power		-0.3	2.16	V
VDD_CPU	CPU Power		-0.3	1.3	V
VDD_GPU	GPU Power		-0.3	1.1	V
VCC_PLL	System PLL Power		-0.3	2.16	V
VCC_DRAM	DRAM Power		-0.3	2.16	V
VDD18_DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
VDD_SYS	Power Supply for System		-0.3	1.1	V
T_{STG}	Storage Temperature		-40	150	°C
Tj	Working Junction Temperature		-40	125	°C
V_{ESD}	ESD Stress Voltage(1)	Human Body Model(HBM)(2)	-2000	2000	V
		Charged Device Model(CDM)(3)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(4)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(5)		Pass		

(1). Electrostatic discharge(ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

(2). Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(3). Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(4). Based on JESD78E; each device is tested with IO pin injection of ±200mA at room temperature.

(5). Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.2. Recommended Operating Conditions

All H616 modules are used under the operating conditions contained in Table 5-2.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	70	°C
Tj	Working Junction Temperature Range	-20	-	110(1)	°C
AVCC	Analog Part Power	1.764	1.8	1.836	V
AC_AVCC	AC Chip Analog Part Power	1.764	1.8	1.836	V
VCC_PC	Digital GPIO C Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PG	Digital GPIO G Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PI	Digital GPIO I Power 1.8V 2.8V 3.3V	 1.62 2.52 2.97	 1.8 2.8 3.3	 1.98 3.08 3.63	V
VCC_IO	GPIO F, GPIO H and System Control Power	2.97	3.3	3.63	V
VCC_USB	USB Analog Power	2.97	3.3	3.63	V
VCC_HDMI	HDMI Power	1.62	1.8	1.98	V
VCC_TV	TV OUT Power	1.78	1.8	1.98	V
VCC_DCXO	DCXO Power	1.62	1.8	1.98	V
VDD_CPU	CPU Power	0.81	-	1.1	V
VDD_GPU	GPU Power	0.81	-	0.99	V
VCC_PLL	System PLL Power	1.62	1.8	1.98	V
VCC_DRAM	DRAM Power DDR4 IO Domain Power LPDDR4 IO Domain Power LPDDR3 IO Domain Power DDR3 IO Domain Power DDR3L IO Domain Power	 1.14 1.06 1.14 1.425 1.283	 1.2 1.1 1.2 1.5 1.35	 1.26 1.17 1.3 1.575 1.45	V
VDD18_DRAM	DRAM 1.8V Internal PAD Power	1.7	1.8	1.98	V
VDD_SYS	Power Supply for System	0.81	-	0.99	V

(1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.

5.3. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

5.4. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of the H616.

Table 5-3. DC Electrical Characteristics (VCC_IO/VCC_PC/VCC_PG/VCC_PI)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC_IO	-	VCC_IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC_IO	V
R_{PU}	Input Pull-up Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
R_{PD}	Input Pull-down Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC_IO – 0.2	-	VCC_IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

NOTE

For PL0~PL1 ports, the R_{PU} and R_{PD} are 4.7kΩ ±20%.
For PC0, PC3~PC7, PF3, PF6, and PG1~PG5 ports, the R_{PU} and R_{PD} are 15kΩ ±20%.
For other GPIO ports, the R_{PU} and R_{PD} are 100kΩ ±20%.

5.5. SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

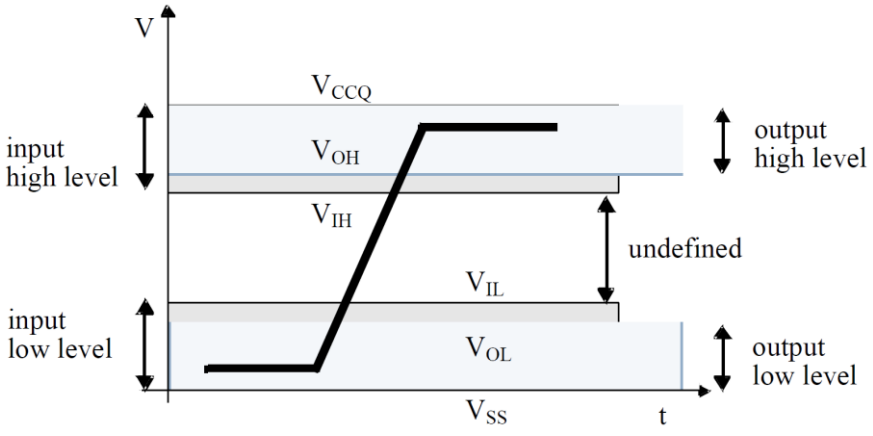


Figure 5-1. SDIO Voltage Waveform

Table 5-4 shows 3.3 V SDIO electrical parameters.

Table 5-4. 3.3 V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V

V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8 V SDIO electrical parameters.

Table 5-5. 1.8 V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6. LRADC Electrical Characteristics

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 2 kHz conversion rate. Table 5-6 lists LRADC electrical characteristics.

Table 5-6. LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	LEVELB(1)	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.266V. For details, see the register description of LRADC in ***Allwinner_H616_User_Manual.***				

5.7. Audio Codec Electrical Characteristics

Test conditions: VDD_SYS = 0.9 V, AVCC=1.8 V, Ta=25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz,16-bit audio data unless otherwise stated.

Table 5-7. Audio Codec Typical Performance

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DACL/DACR to LINEOUTL/R(R=10kΩ)**					
	Full-scale Level	0dBFS 1kHz	-	0.56	-	Vrms
	SNR(A-weighted)	0data	-	92	-	dB
	THD+N	0dBFS 1kHz	-	-80	-	dB
	Noise	0data	-	12	-	uV

5.8. Clock Electrical Characteristics

5.8.1. Input Clock Requirements

The H616 has two clock inputs. Each clock input passes through an internal oscillator which can be connected to an external crystal.

The 24 MHz oscillator provides a 24 MHz reference clock which is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through DXIN. Table 5-8 lists the recommended values of 24 MHz crystal.

Table 5-8. 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24	-	MHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-

5.9. External Memory Electrical Characteristics

5.9.1. Nand AC Electrical Characteristics

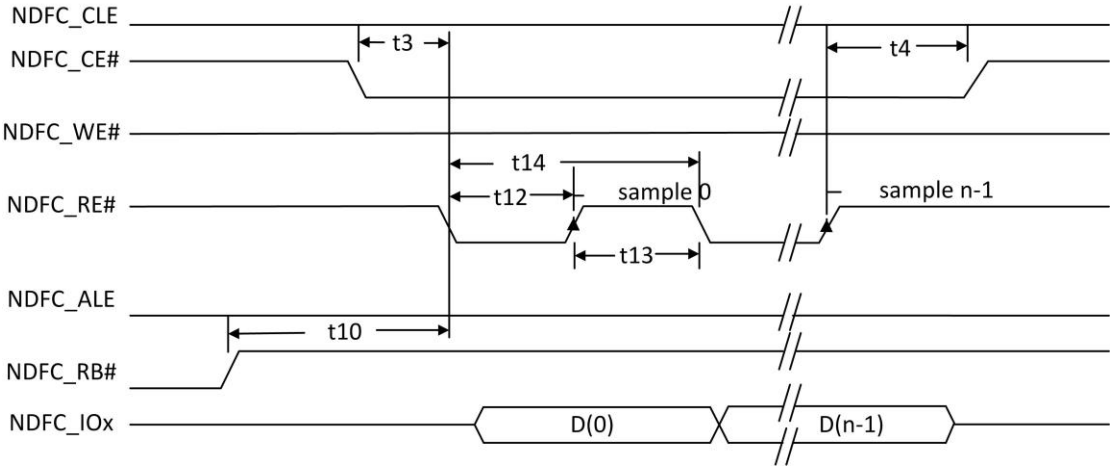


Figure 5-2. Conventional Serial Access Cycle Timing (SAM0)

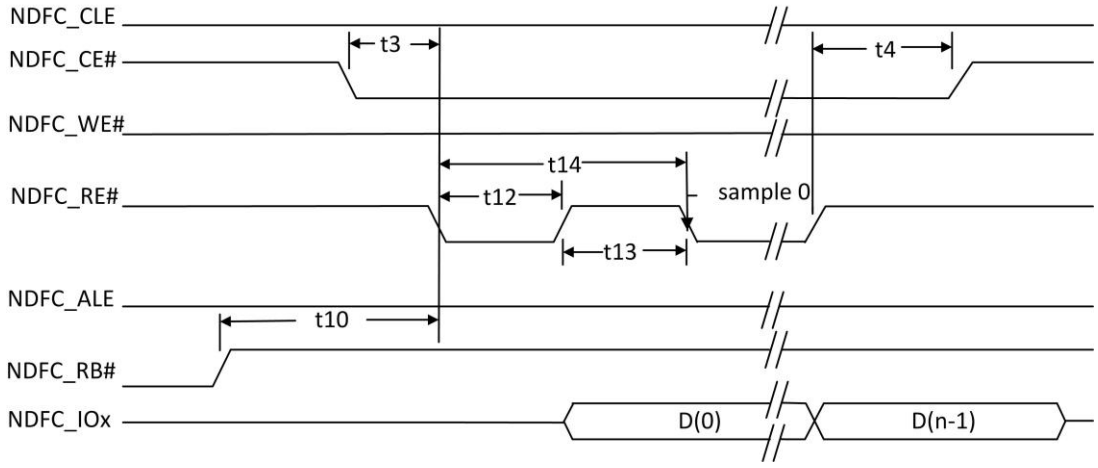


Figure 5-3. EDO Type Serial Access after Read Cycle Timing (SAM1)

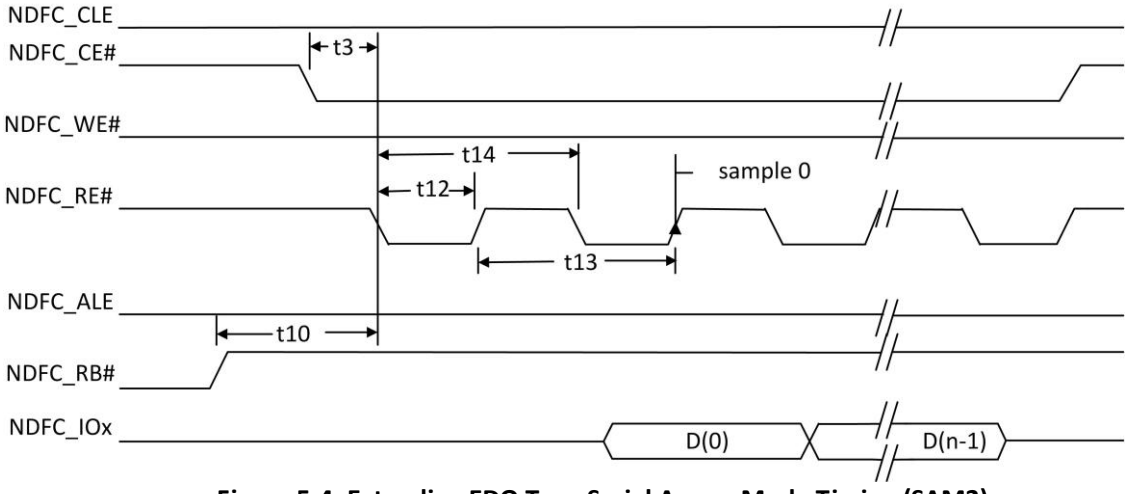


Figure 5-4. Extending EDO Type Serial Access Mode Timing (SAM2)

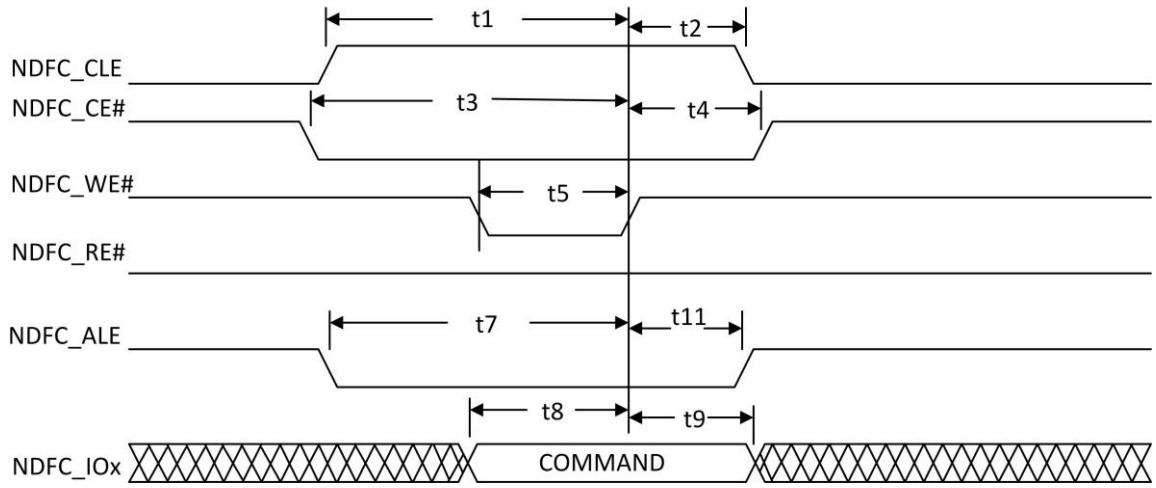


Figure 5-5. Command Latch Cycle Timing

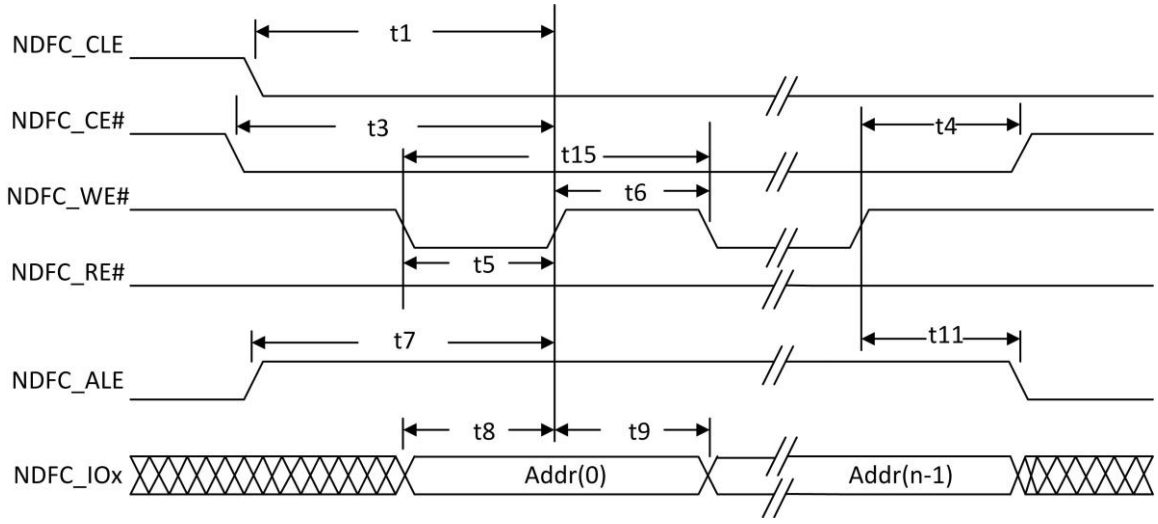


Figure 5-6. Address Latch Cycle Timing

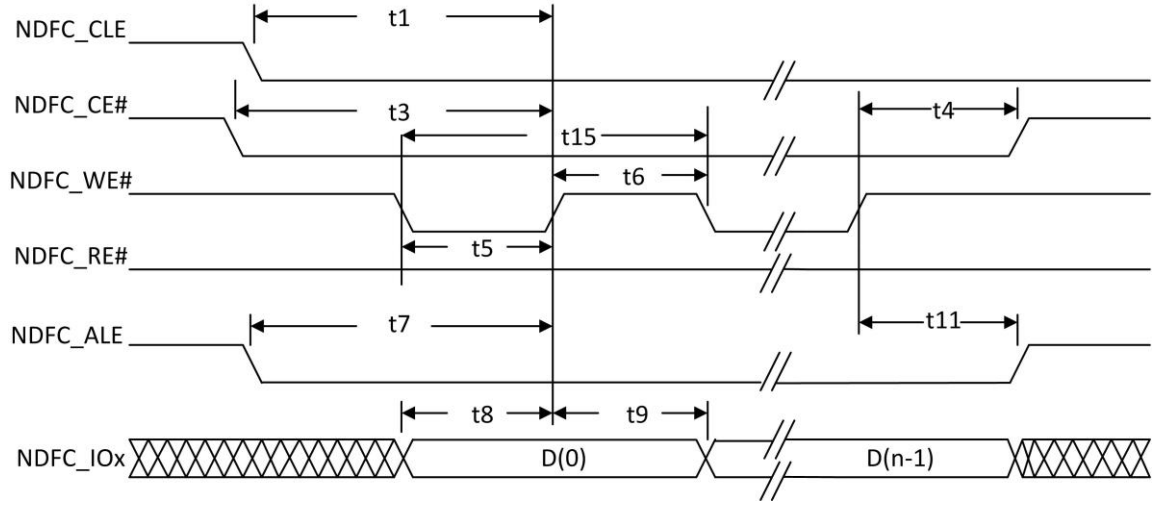


Figure 5-7. Write Data to Flash Cycle Timing

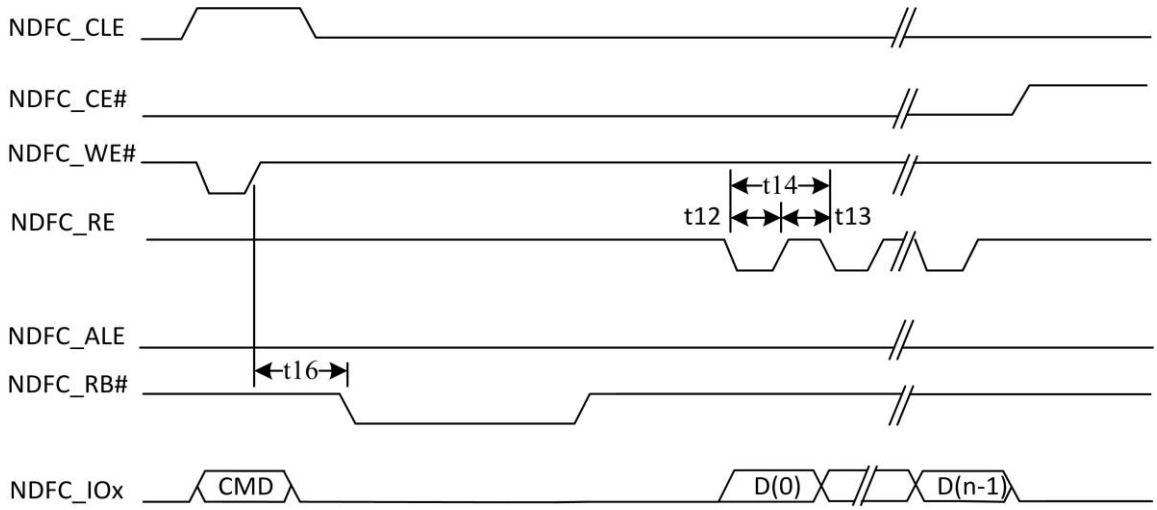


Figure 5-8. Waiting R/B# Ready Timing

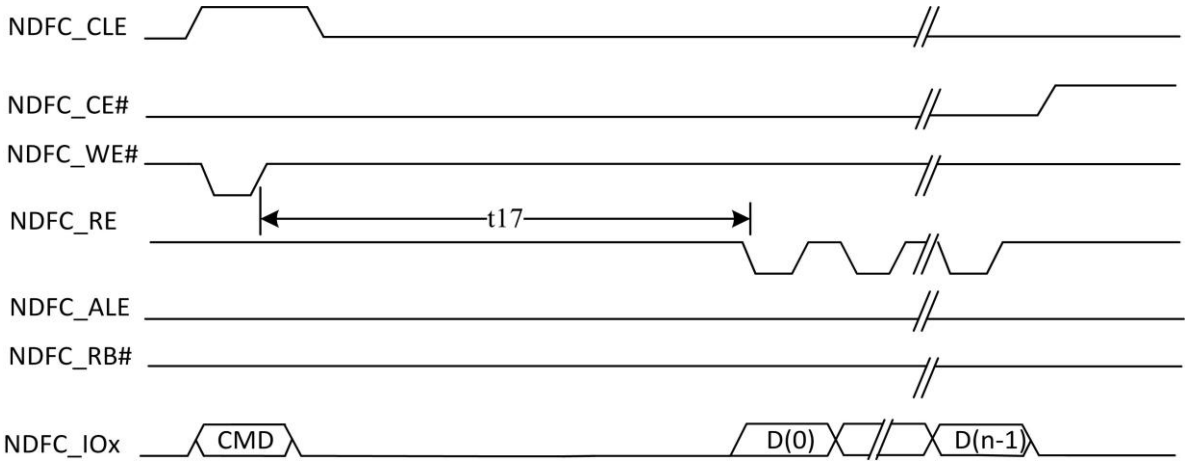


Figure 5-9. WE# High to RE# Low Timing

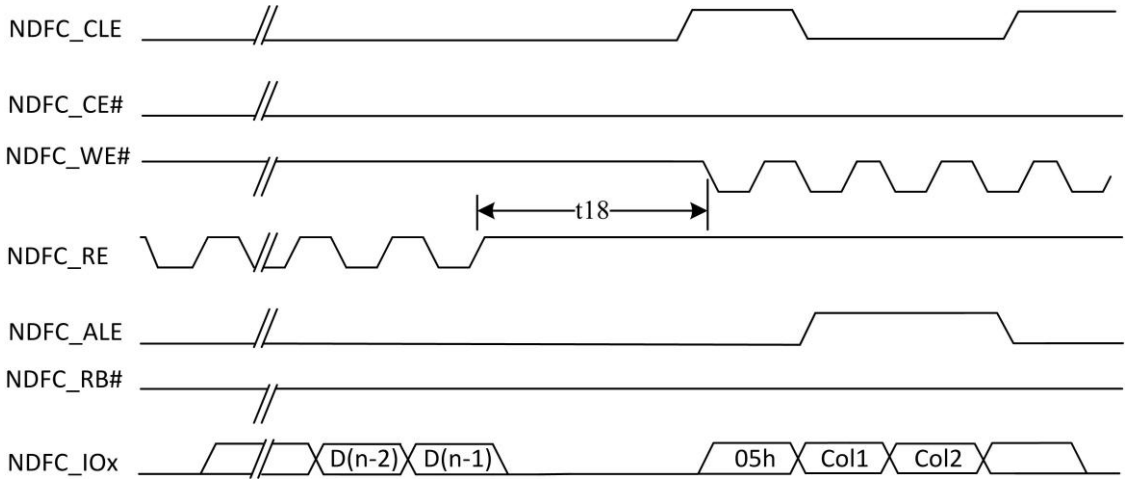


Figure 5-10. RE# High to WE# Low Timing

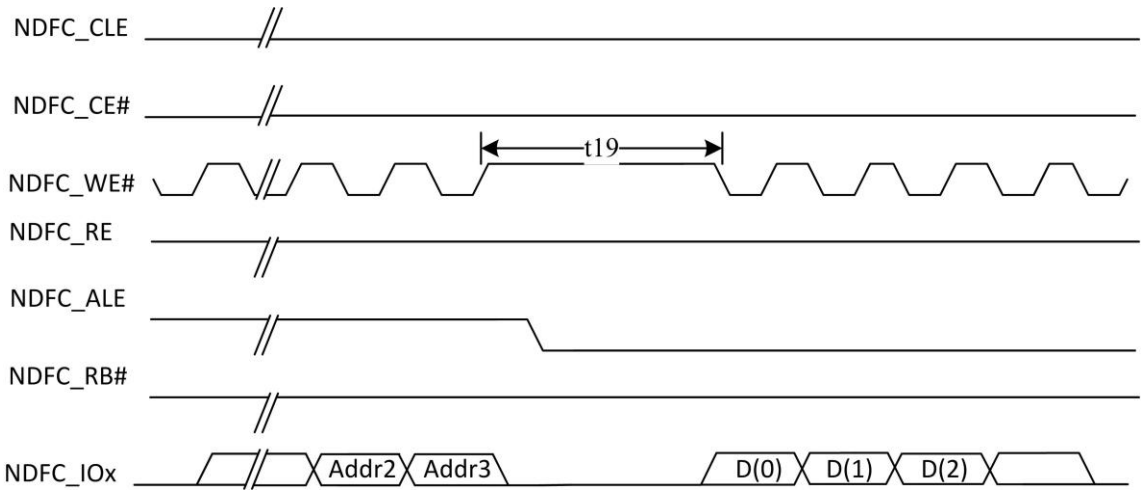


Figure 5-11. Address to Data Loading Timing

Table 5-9. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T(1)	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns
(1):T is the cycle of internal clock. **(2),(3),(4),(5): This values is configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.**			

5.9.2. SMHC AC Electrical Characteristics

5.9.2.1. SMHC0/1

(1) SDR Mode(<100 MHz)

The contents of this section can be applied to DS, HS, SDR12, SDR25, SDR50, SDR104(<100 MHz) speed mode.

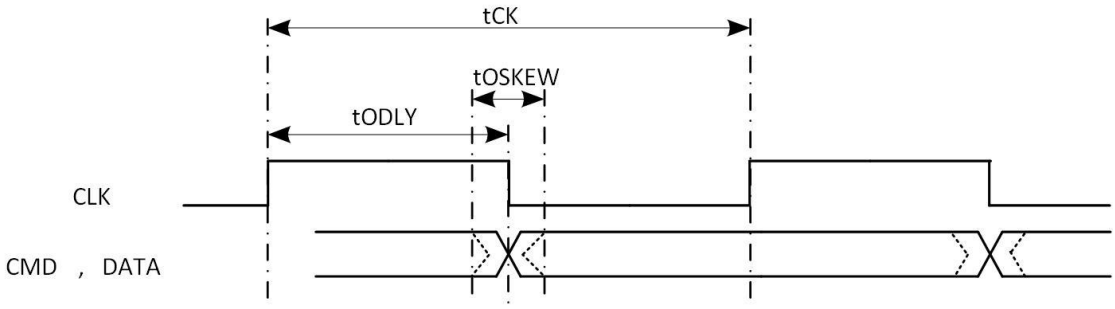


Figure 5-12. SMHC0/1 SDR Mode Output Timing Diagram

Table 5-10. SMHC0/1 SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.625	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

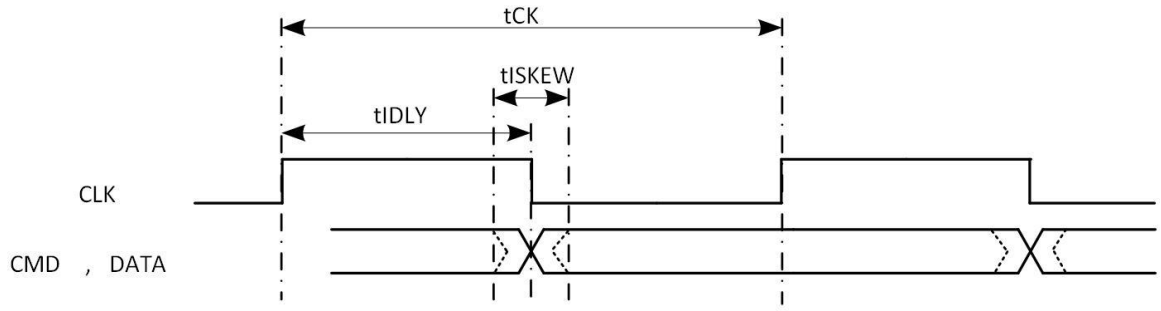


Figure 5-13. SMHC0/1 SDR Mode Input Timing Diagram

Table 5-11. SMHC0/1 SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
NOTE (1): The driver strength level of GPIO is 2 for test.					

(2) DDR50 Mode

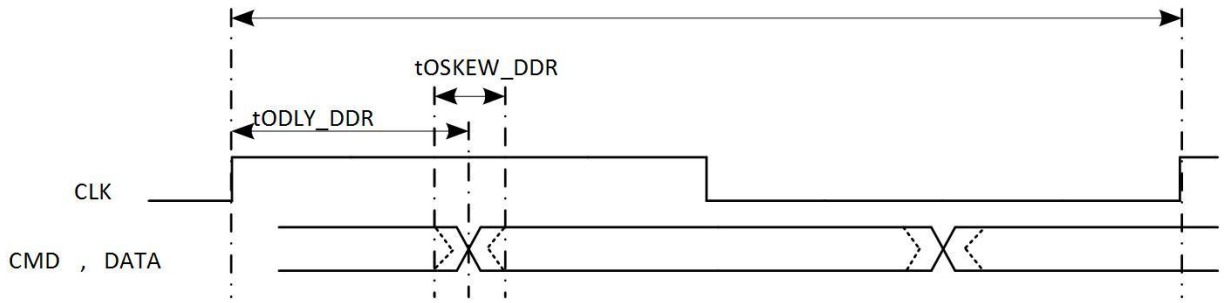


Figure 5-14. SMHC0/1 DDR50 Mode Output Timing Diagram

Table 5-12. SMHC0/1 DDR50 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.884	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

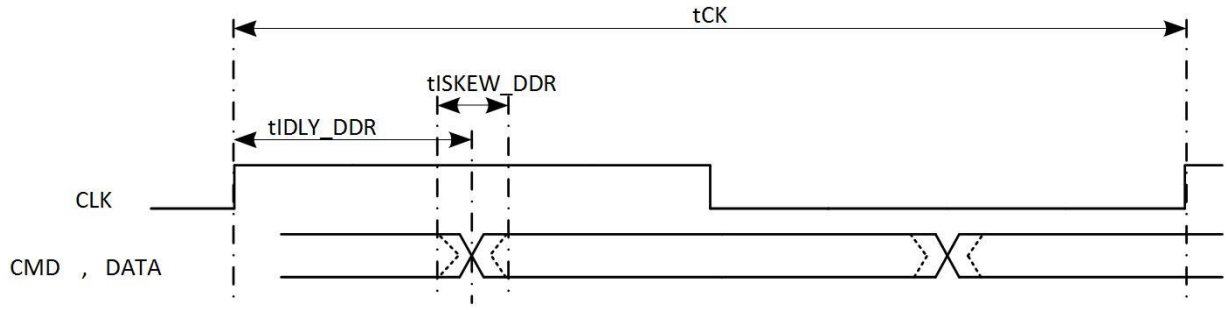


Figure 5-15. SMHC0/1 DDR50 Mode Input Timing Diagram

Table 5-13. SMHC0/1 DDR50 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-c	8.3	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns
NOTE (1): The driver strength level of GPIO is 2 for test.					

(3) SDR104 Mode(>100 MHz)

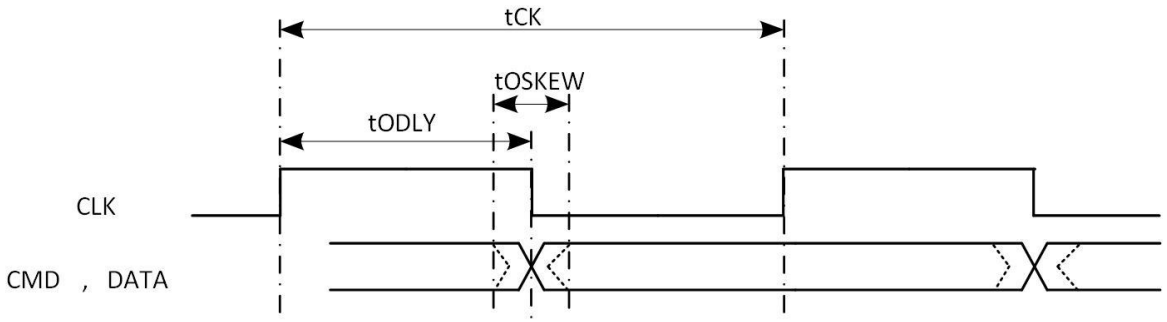


Figure 5-16. SMHC0/1 SDR104 Mode Output Timing Diagram

Table 5-14. SMHC0/1 SDR104 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

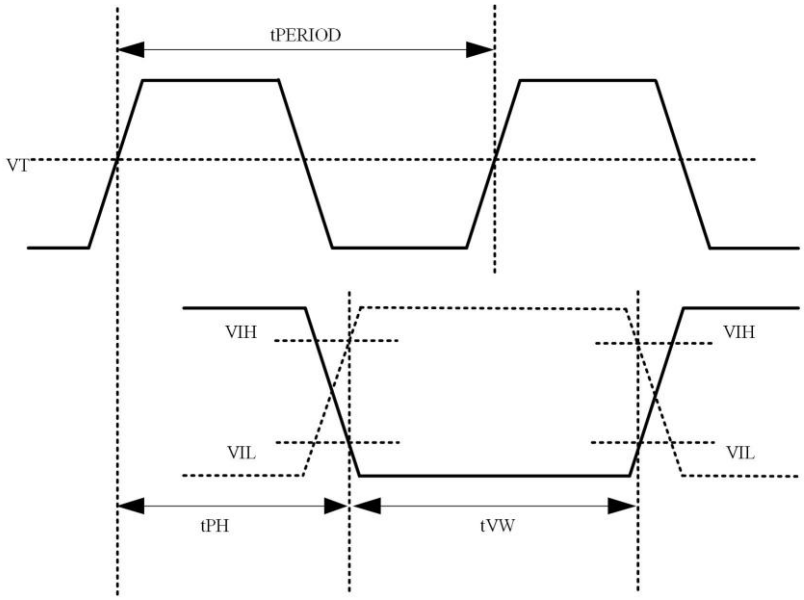


Figure 5-17. SMHC0/1 SDR104 Mode Input Timing Diagram

Table 5-15. SMHC0/1 SDR104 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz.						

NOTE (2): The driver strength level of GPIO is 3 for test. **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**

5.9.2.2. SMHC2

(1) HS-SDR/HS-DDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

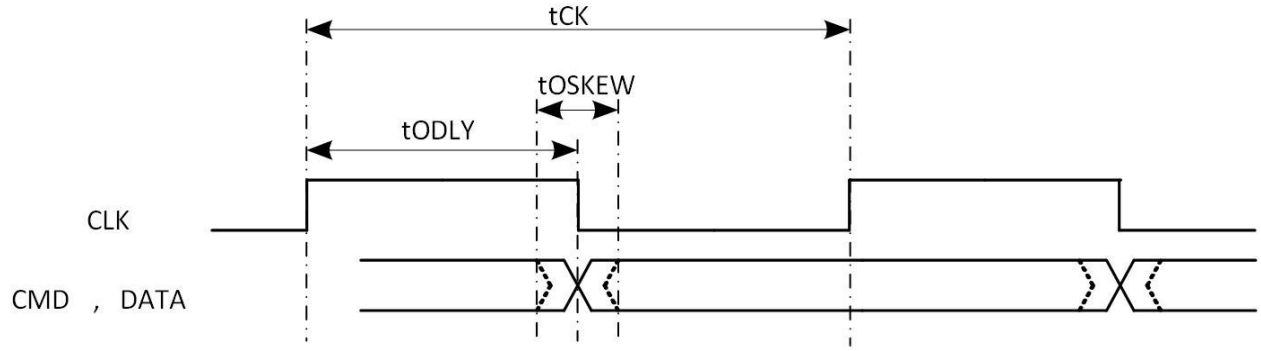


Figure 5-18. SMHC2 HS-SDR Mode Output Timing Diagram

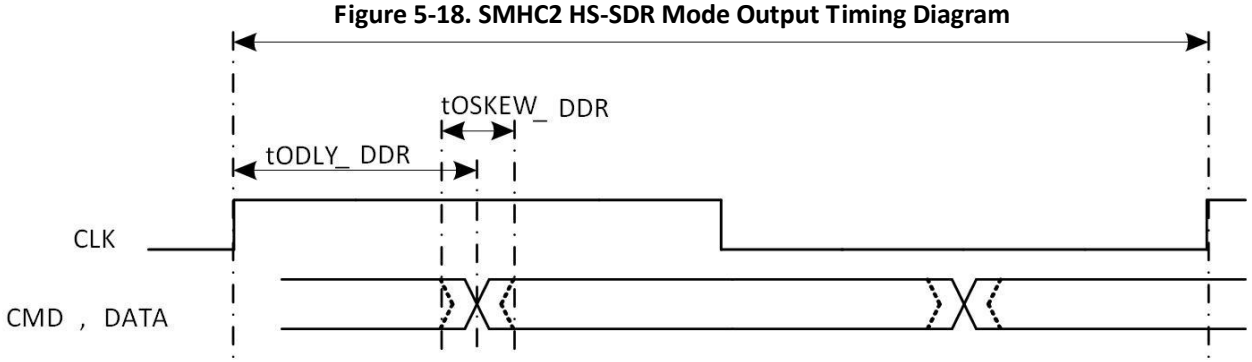


Figure 5-19. SMHC2 HS-DDR Mode Output Timing Diagram

Table 5-16. SMHC2 HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**						

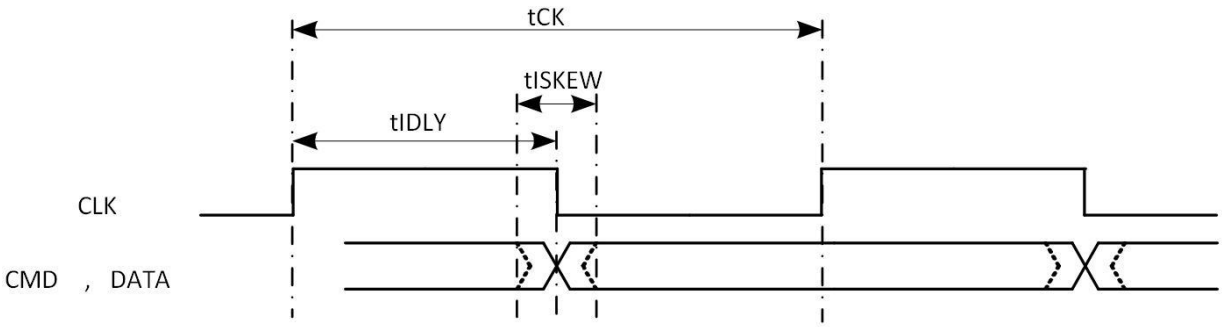


Figure 5-20. SMHC2 HS-SDR Mode Input Timing Diagram

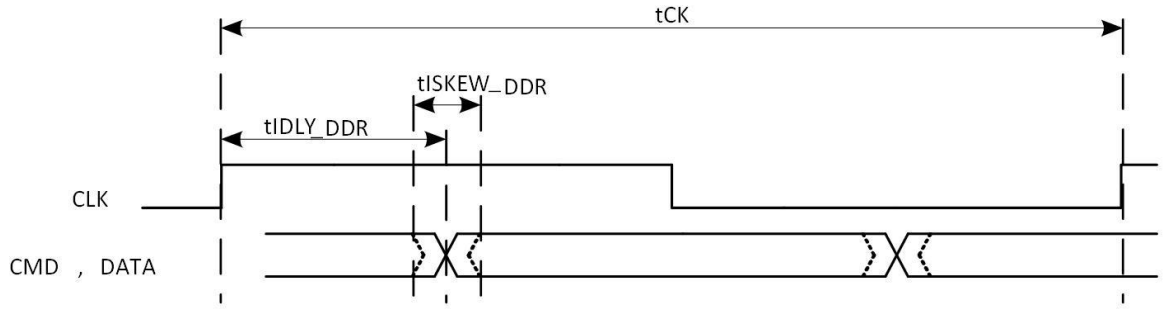


Figure 5-21. SMHC2 HS-DDR Mode Input Timing Diagram

Table 5-17. SMHC2 HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns	
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	8.3	ns	
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns	
NOTE (1): The driver strength level of GPIO is 2 for test.						

(2) HS200 Mode

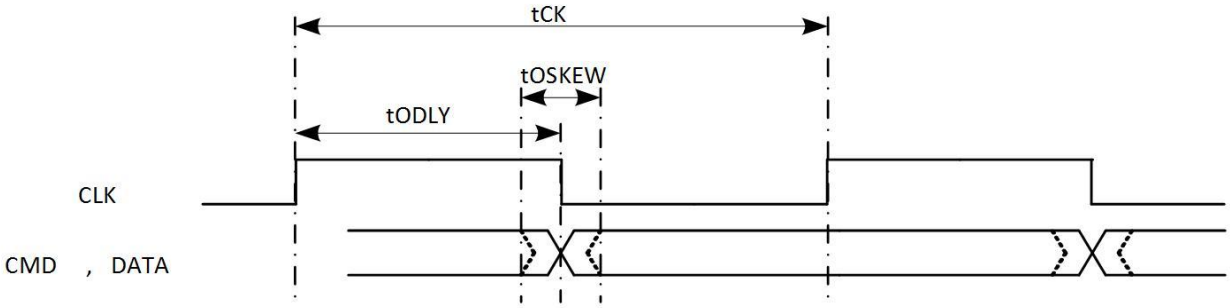


Figure 5-22. SMHC2 HS200 Mode Output Timing Diagram

Table 5-18. SMHC2 HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark

CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

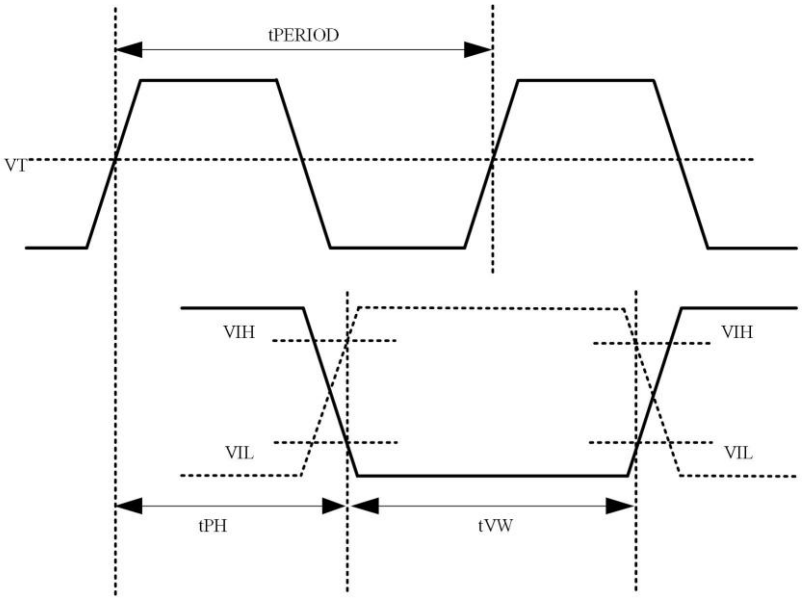


Figure 5-23. SMHC2 HS200 Mode Input Timing Diagram

Table 5-19. SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, DATA valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.** **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**						

(3) HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

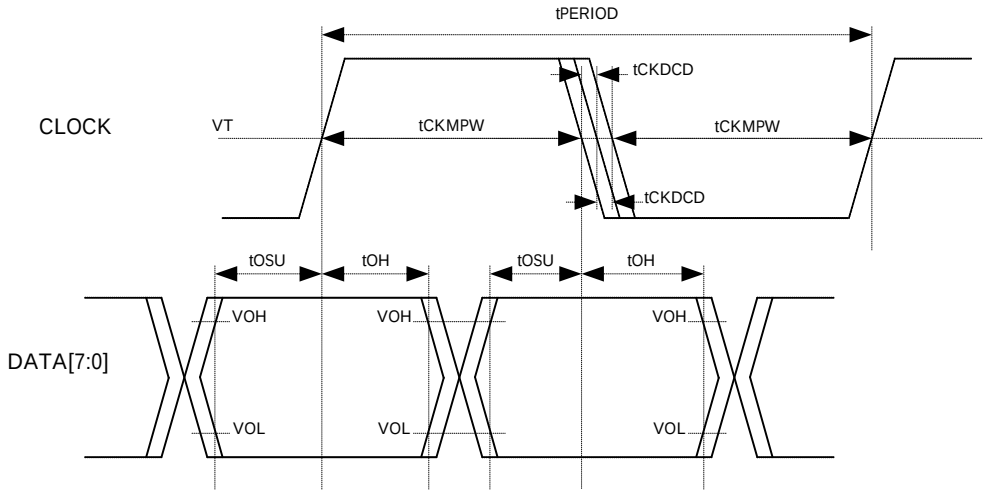


Figure 5-24. SMHC2 HS400 Mode Data Output Timing Diagram

Table 5-20. SMHC2 HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

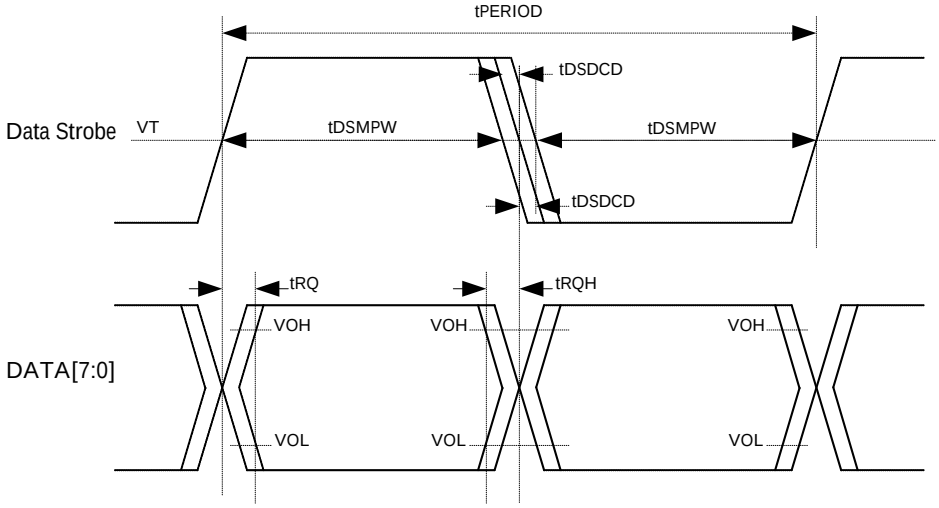


Figure 5-25. SMHC2 HS400 Mode Data Input Timing Diagram

Table 5-21. SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	

Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

5.10. External Peripheral Electrical Characteristics

5.10.1. EMAC AC Electrical Characteristics

5.10.1.1. RMII

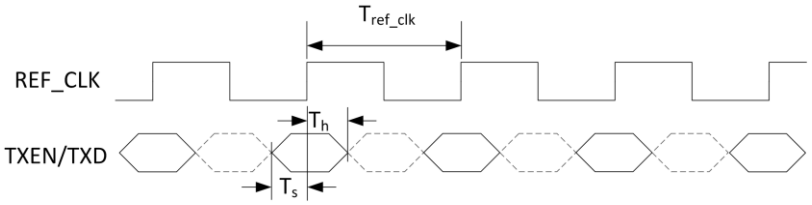


Figure 5-26. RMII Interface Transmit Timing

Table 5-22. RMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	Ts	4	-	-	ns
TXD/TXEN to REF_CLK hold time	Th	2	-	-	ns

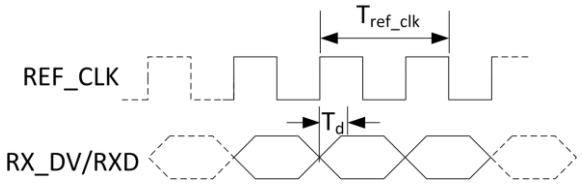


Figure 5-27. RMII Interface Receive Timing

Table 5-23. RMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
REF_CLK rising edge to RX_DV/RXD	Td	-	10	12	ns

5.10.1.2. RGMII

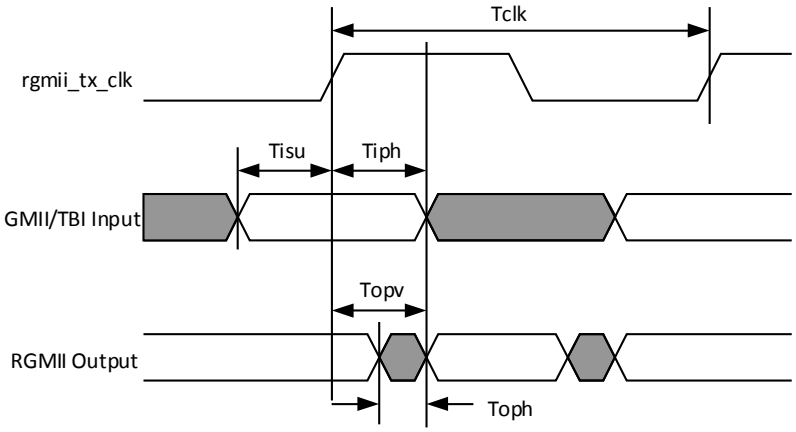


Figure 5-28. RGMII Interface Transmit Timing

Table 5-24. RGMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_tx_clk clock period	Tclk	8	-	DC	ns
RGMII/TBI input set up prior to rgmii_tx_clk	Tisu	2.8	-	-	ns
RGMII/TBI input data hold after rgmii_tx_clk	Tiph	0.1	-	-	ns
RGMII output data valid after rgmii_tx_clk	Topv	-	-	0.85	ns
RGMII output data hold after rgmii_tx_clk	Toph	0	-	-	ns

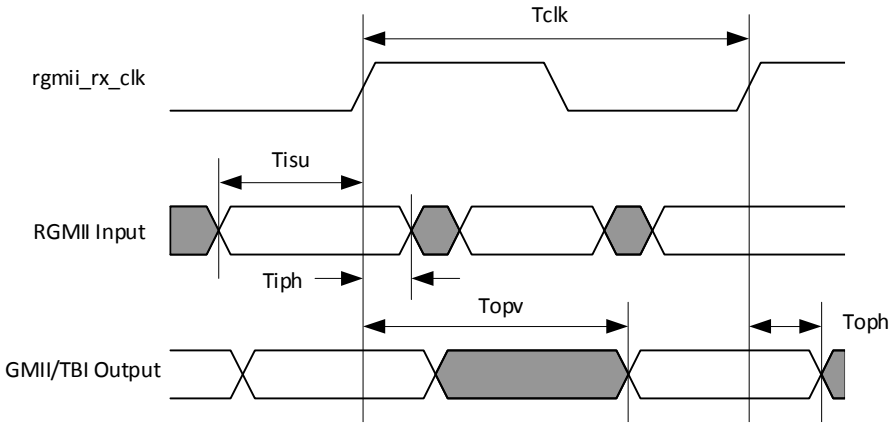


Figure 5-29. RGMII Interface Receive Timing

Table 5-25. RGMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_rx_clk clock period	Tclk	8	-	DC	ns
RGMII input set up prior to rgmii_rx_clk	Tisu	2.6	-	-	ns
RGMII input data hold after rgmii_rx_clk	Tiph	0.8	-	-	ns
GMII/TBI input data valid after rgmii_rx_clk	Topv	-	-	5.2	ns
GMII output data hold after rgmii_rx_clk TBI output data hold after rgmii_rx_clk	Toph	0.1 0.5	-	-	ns

5.10.2. CIR-RX AC Electrical Characteristics

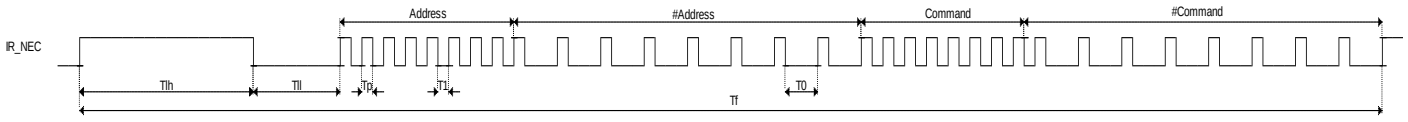


Figure 5-30. CIR-RX Timing

Table 5-26. CIR-RX Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

5.10.3. SPI AC Electrical Characteristics

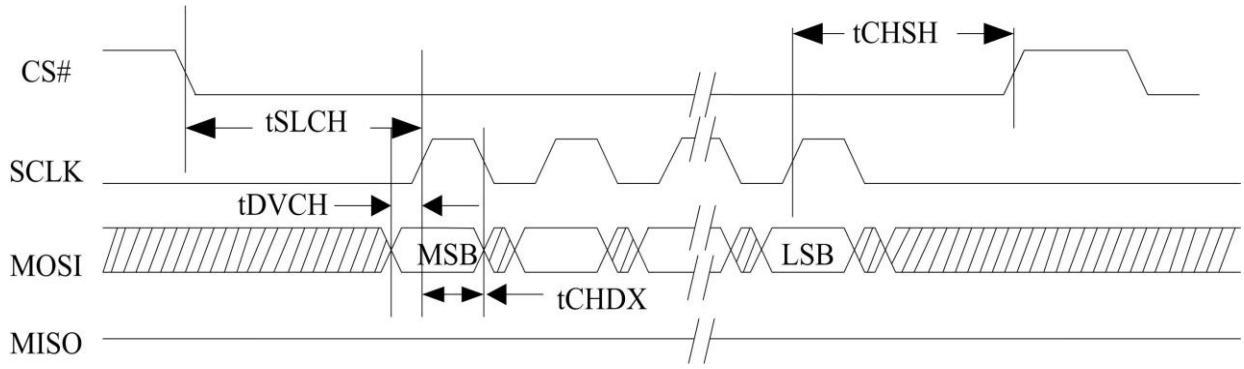


Figure 5-31. SPI MOSI Timing

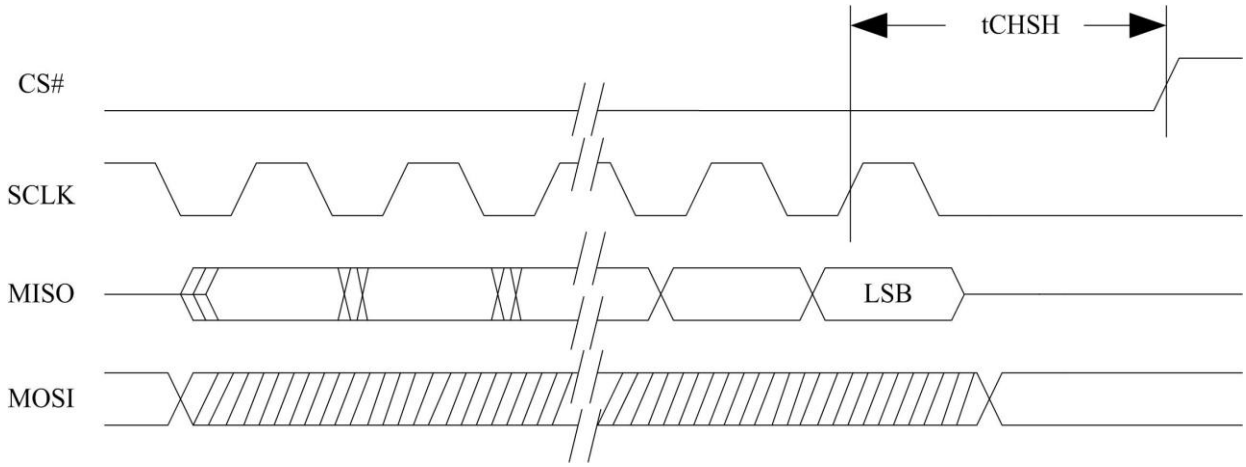


Figure 5-32. SPI MISO Timing

Table 5-27. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T(1)	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
NOTE (1):T is the cycle of clock.					

5.10.4. UART AC Electrical Characteristics

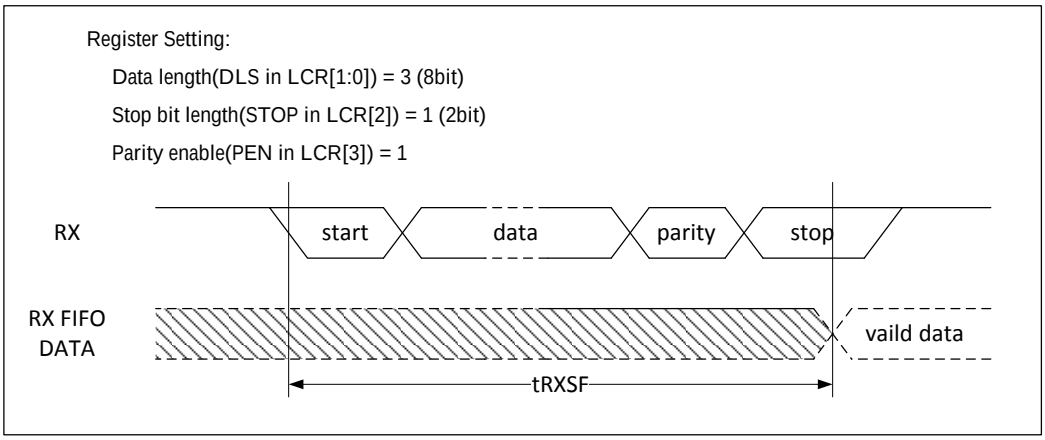


Figure 5-33. UART RX Timing

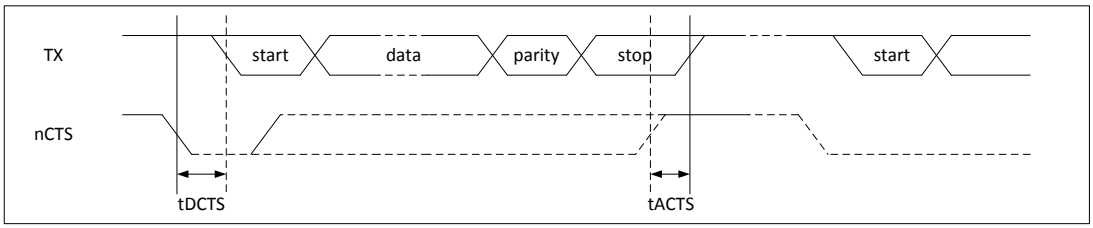


Figure 5-34. UART nCTS Timing

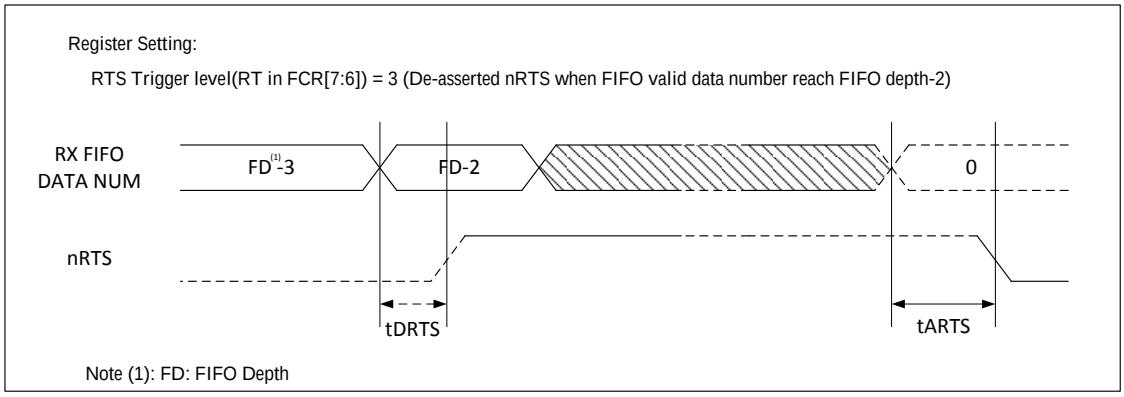


Figure 5-35. UART nRTS Timing

Table 5-28. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
NOTE (1): BRP(Baud-Rate Period).					

5.10.5. TWI AC Electrical Characteristics

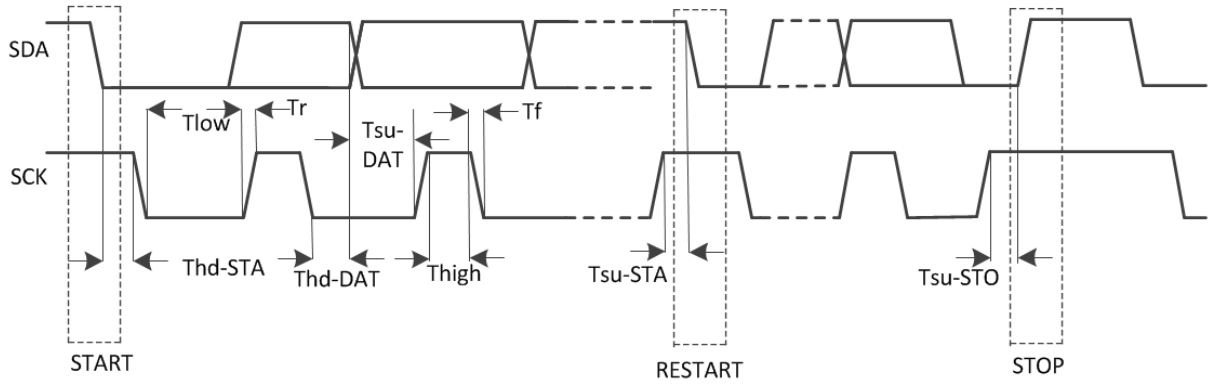


Figure 5-36. TWI Timing

Table 5-29. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	

SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

5.10.6. TSC AC Electrical Characteristics

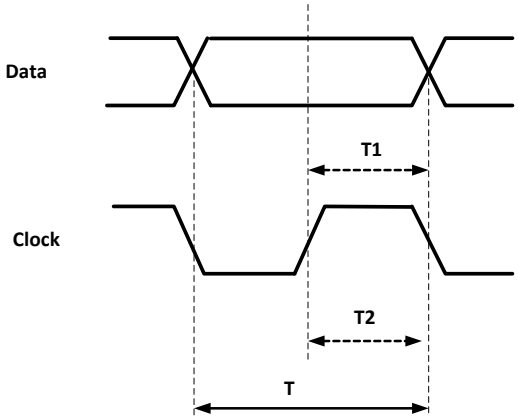


Figure 5-37. TSC Data and Clock Timing

Table 5-30. TSC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Data hold time	T1	$T^{[1]}/2-T^{[1]}/10$	$T^{[1]}/2$	$T^{[1]}/2+T^{[1]}/10$	us
Clock pulse width	T2	$T^{[1]}/2-T^{[1]}/10$	$T^{[1]}/2$	$T^{[1]}/2+T^{[1]}/10$	us
NOTE (1): T is the cycle of clock.					

5.10.7. I2S/PCM AC Electrical Characteristics

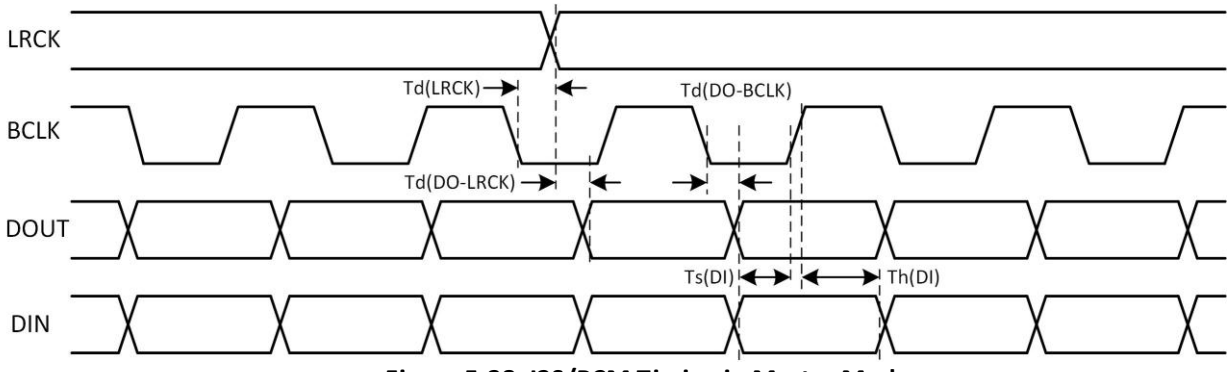


Figure 5-38. I2S/PCM Timing in Master Mode

Table 5-31. I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns

DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

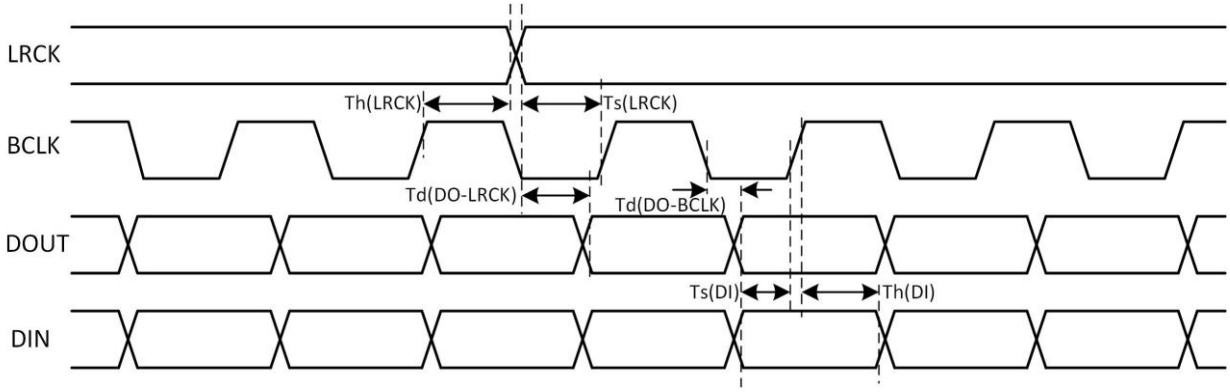


Figure 5-39. I2S/PCM Timing in Slave Mode

Table 5-32. I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.10.8. DMIC AC Electrical Characteristics

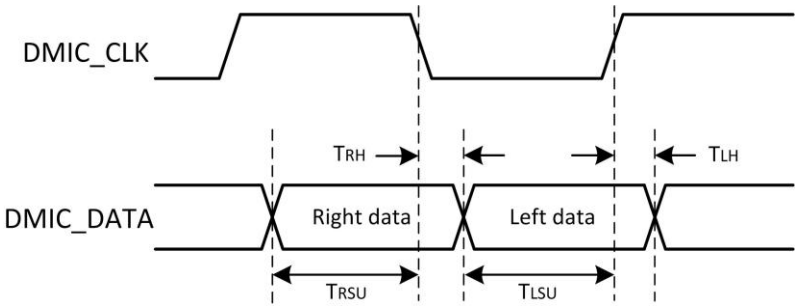


Figure 5-40. DMIC Timing

Table 5-33. DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) setup time to falling edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) hold time from falling edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) setup time to rising edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) hold time from rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

5.10.9. OWA AC Electrical Characteristics

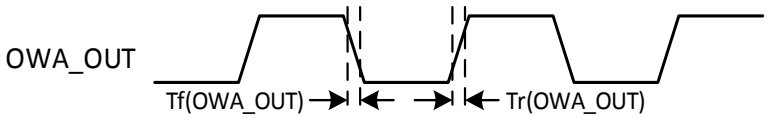


Figure 5-41. OWA Timing

Table 5-34. OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns

5.11. Power-On and Power-Off Sequence

5.11.1. Power-On Sequence

Figure 5-42 shows an example of the power on sequence for the H616 device. The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- No sequence requirement between power domains which are grouped as shown in the following example sequence.
- VCC_IO and VCC_PLL start to ramp up at the same time to avoid the electric leakage between 1.8 V and 3.3 V.
- T4 >= 0 ms: VCC_DRAM must be stable later than VDD18_DRAM.
- T1 >= 8 ms: VDD_SYS is recommended to ramp up at least 8 ms later than VCC_PLL.
- T2 >= 8 ms: After all of the preceding powers have stabilized with a minimum delay of 8 ms, the RESET can be released.
- T3 >= 4 ms: 24 MHz clock starts oscillating and be stable at least 4 ms later than RESET.

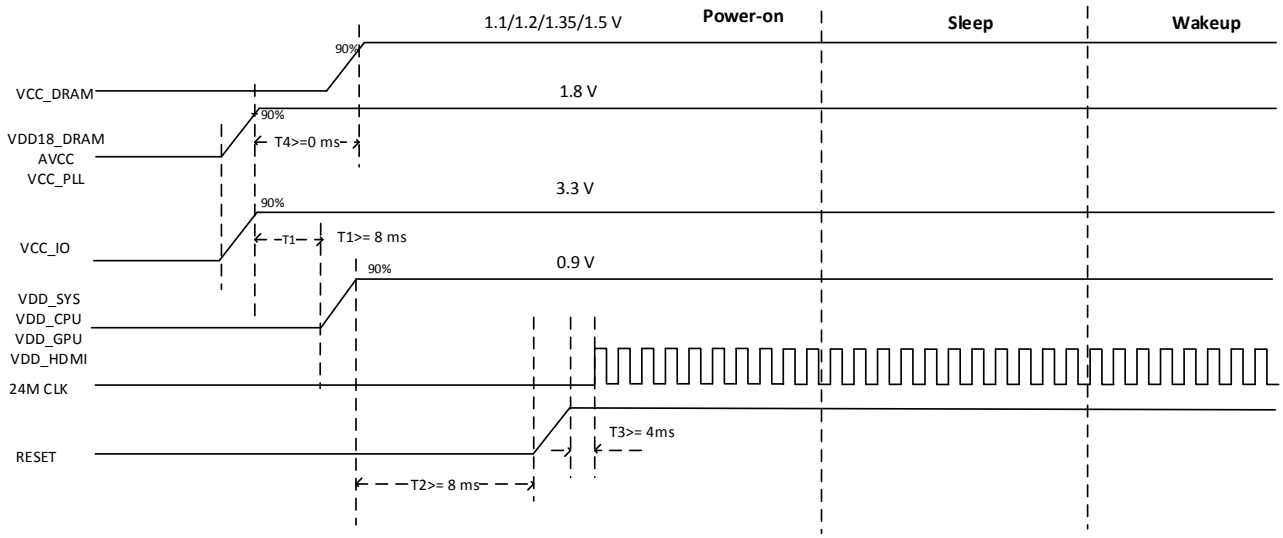


Figure 5-42. Power On Timing

5.11.2. Power-Off Sequence

No special restrictions.

6. Package Thermal Characteristics

Table 6-1 shows thermal resistance parameters of the H616. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board, natural convection, no air flow.

Table 6-1. H616 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	27.26	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	15.4	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	13.47	-	°C/W

7. Pin Assignment

7.1. Pin Map

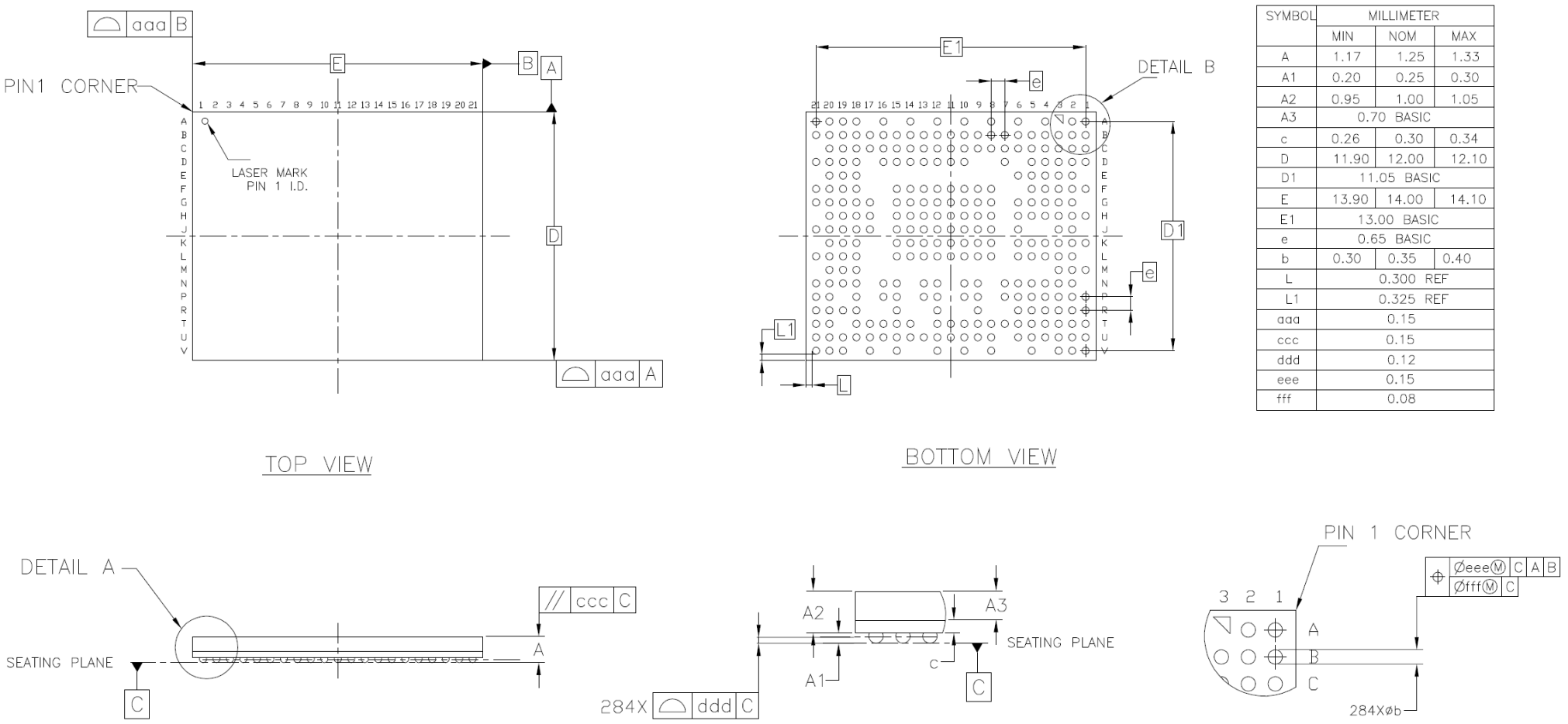
For H616, TFBGA 284 balls, 14 mm x 12 mm, 0.65 mm pitch package is offered. The pin map is illustrated in Figure 7-1 for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A	GND	PG18		PG6		PG0		PG15		GND		PH9		PH4		RESET		GND	EPHY_TXP	EPHY_TXN	GND
B	PC0	PG19	PG9	PG7	PG3	GND	PG5	PG16	PG14	PG11	DXIN	PH7	PH10	PH5	PH2	GND	FEL	PL1	EPHY_RTX	EPHY_RXP	EPHY_RXN
C	PC2	PC1	PG17	PG8	PG4	PG2	PG1	PG10	PG12	PG13	REFCLK_OUT	DXOUT	PH8	PH6	PH3	JTAG_SEL	AC_VRA1	PL0	HTX2P	HTX2N	
D	PC3	PC4	PC5	PI1	PI9		VCC_PG			VCC_IO	VCC_DCXO	VCC_PLL	DXLDO_OUT	PLLTEST	PH1	PH0		AC_AVCC	GND	HTX1P	HTX1N
E		PC6	PC8	PI3	PI13	PI8												VCC_EPHY	HTX0P	HTX0N	
F	PC9	PC10	PC11	PC7	VCC_PC			VDD_GPUFB	VDD_GPU	VDD_GPU	VDD_SYS	VDD_SYS	VDD_SYS	GND	GND			VCC_HDMI	HSCL	HTXCP	HTXCN
G		PC12	PC13	PI7	PI4	PI2		VDD_GPU	VDD_GPU	VDD_SYS	VDD_SYS	VDD_SYS	GND	GND	GND		HCEC	HHPD	LINEOUTL	LINEOUTR	HSDA
H	PC14	PC15	PC16	PI5	PI6	PI0		VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	GND		AVCC	AGND	GND	VCC_TV	
J		PF0	PF1			VCC_PI		VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	GND	GND	GND	GND		VRA2	VRA1	USB0_DM	USB0_DP	TV_OUT
K	PF2	PF6	PF3	PI11	PI12	PI16		GND	GND	GND	GND	GND	GND	GND	GND			REXT	USB2_DM	USB2_DP	
L		PF4	PF5	PI15	PI10	PI14		VDD_CPUFB	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VDD18_DRAM	SZQ			LRADC	USB3_DM	USB3_DP	GND
M	GND	GND	GND															VCC_USB	USB1_DM	USB1_DP	
N		SDQ2	SDQ0	SDQ13	SDQ15	GND	SDQ26		GND	SDQM3		GND	SA15		GND	SA9		GND	SA7	SODT1	SBA0
P	SDQ5	SDQ7	GND	SDQ10	SDQ8	SDQ14	SDQ25		SDQ27	SDQ28		SDQ30	SCKE1		SA5	SA13		SACT		SBG0	SBG1
R	SDQS0N	SDQS0P	SDQM1	SDQ11	GND	SDQ12			SDQ24			SDQ31			SBA1			SA4	SA10	SCS1	GND
T	GND	SDQ6	GND	SDQ3	SDQ23	SDQ20	SDQ22	GND	SDQM2	GND	SDQ16	SDQ18		SCKP	GND	SA3	GND	SA2		SODT0	SA0
U	SDQM0	SDQS1P	SDQ4	SDQ1	SDQ21	GND		SDQS2N	SDQ19	SDQS3N	SDQ29	SDQ17	GND	SCKN	SA11	SA12	SA1	SA16	SA8	SA6	SRST
V	GND	SDQS1N	SDQ9		GND			SDQS2P		SDQS3P		GND			SCKE0		SCS0		GND	SA14	GND

Figure 7-1. H616 Pin Map

7.2. Package Dimension

Figure 7-2 shows the top, bottom, and side views of H616 package dimension.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.17	1.25	1.33
A1	0.20	0.25	0.30
A2	0.95	1.00	1.05
A3	0.70 BASIC		
c	0.26	0.30	0.34
D	11.90	12.00	12.10
D1	11.05 BASIC		
E	13.90	14.00	14.10
E1	13.00 BASIC		
e	0.65 BASIC		
b	0.30	0.35	0.40
L	0.300 REF		
L1	0.325 REF		
aaa	0.15		
ccc	0.15		
ddd	0.12		
eee	0.15		
fff	0.08		

Figure 7-2. H616 Package Dimension

8. Carrier, Storage and Baking Information

8.1. Carrier

8.1.1. Matrix Tray Information

Table 8-1 shows the H616 matrix tray carrier information.

Table 8-1. Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 136 mm x 7.62 mm	119 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12 mm x 180 mm x 85 mm Front-Back:12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

HIC :

Desiccant :

RoHS symbol:

Product label:

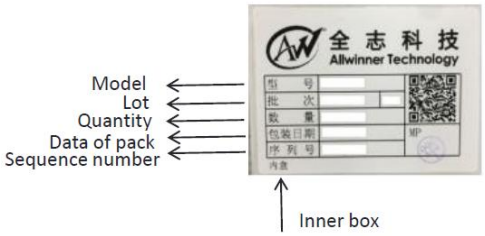
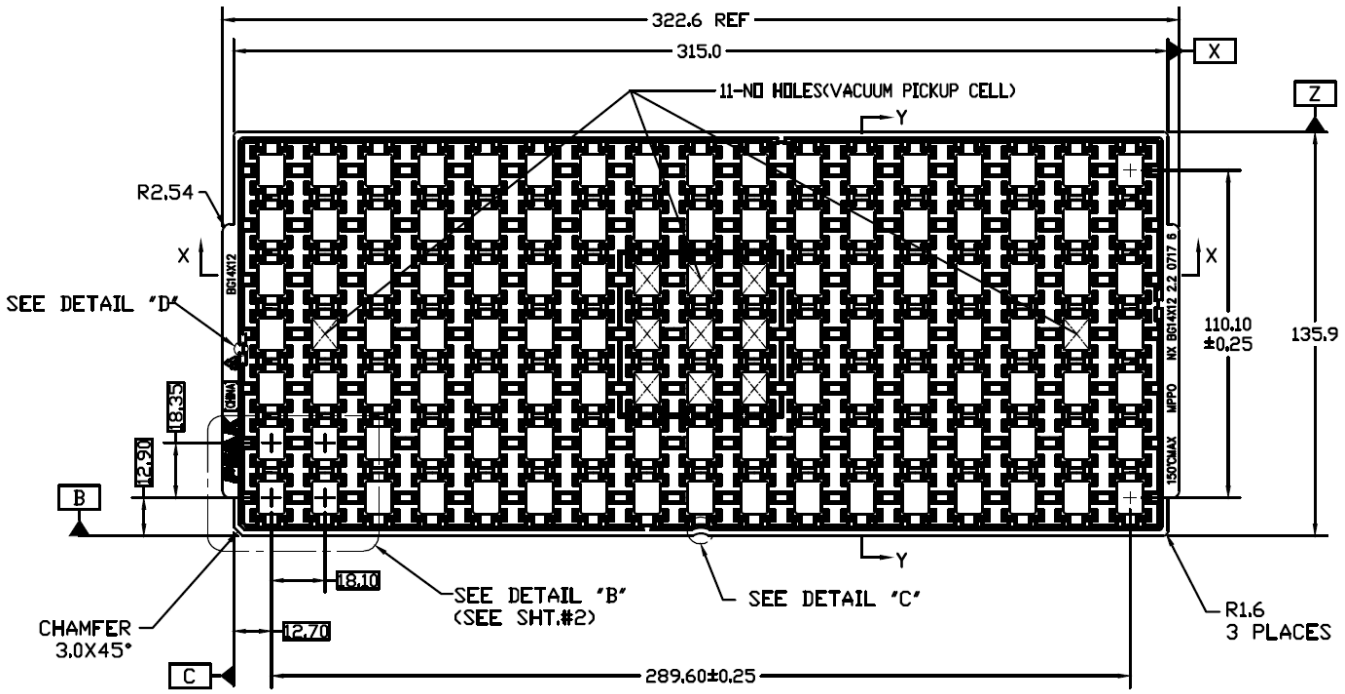


Table 8-2 shows the H616 packing quantity.

Table 8-2. Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
H616	14x12	119	10	1190	6	7140

Figure 8-1 shows tray dimension drawing of the H616.



NOTES:

1. MATERIAL - MPPO
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TOLERANCES X.X=±0.25
   X.XX=±0.13
   UNLESS OTHERWISE SPECIFIED.
4. ESD - SURFACE RESISTIVITY
   $-1X10^{5} \leq \rho < 1X10^{10}$ OHMS/SQ.
5. FOR PACKAGE - BG14X12
6. PART NO. :NX BG14X12 2.2 0717 6
   (PLEASE INDICATE ON PURCHASE ORDER).
7. DATECODE AT TRAY BOTTOM SIDE.
8. Matrix:17X7=119.

Figure 8-1. Tray Dimension Drawing

8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1. Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL is defined in Table 8-3.

Table 8-3. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The H616 device samples are classified as MSL3.

8.2.2. Bagged Storage Conditions

The shelf life of the H616 device samples is defined in Table 8-4.

Table 8-4. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

8.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the H616 are as follows.

Table 8-5. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

8.3. Baking

It is not necessary to bake the H616 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the H616 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake the H616 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the sample baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

9. Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The appropriate reflow conditions are defined in Figure 9-1 and Table 9-1.

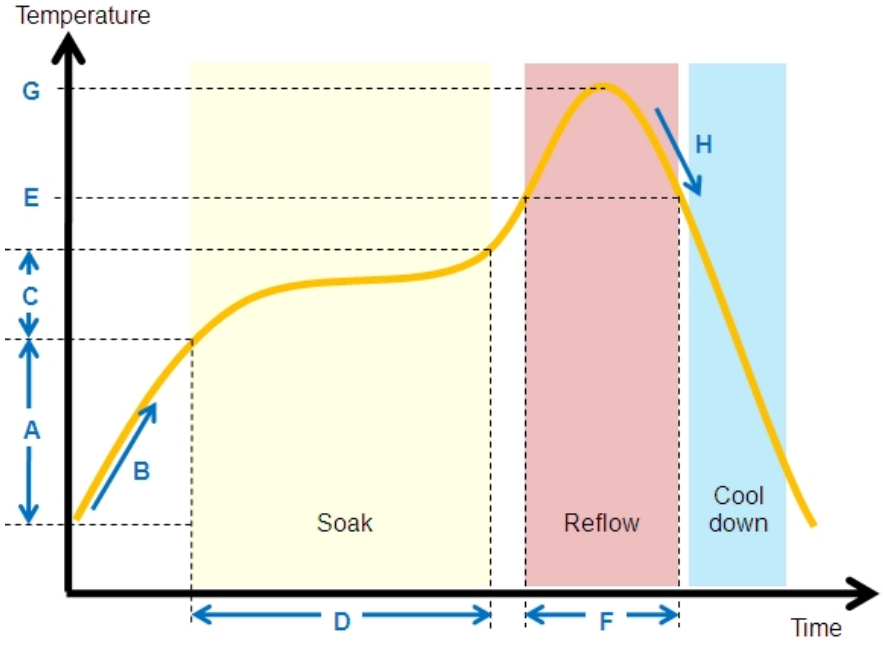


Figure 9-1. Lead-free Reflow Profile

Table 9-1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

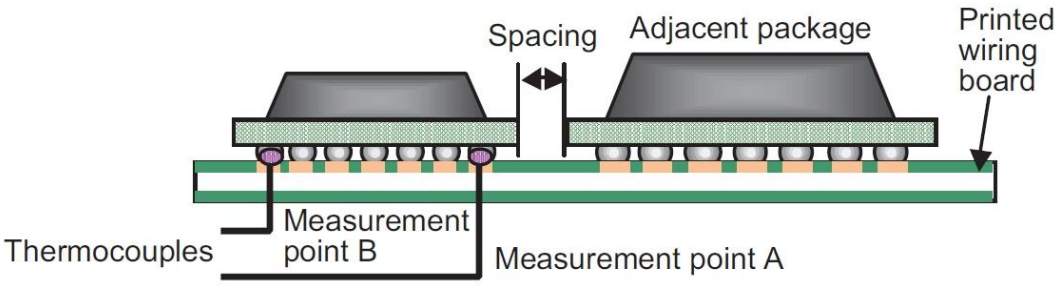


Figure 9-2. Measuring the Reflow Soldering Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10. FT and IQC Test

10.1. FT Test

FT test includes two parts, module verification and linux system testing. For module verification, it verifies the logic function of each module; for linux system testing, it mainly tests CPU, DDR, memory test and linpack, etc. The linux system testing can cover areas where module verification does not cover, with the goal of increasing coverage as much as possible.

10.2. IQC Test

IQC test system is used for sampling inspection before delivery, it is the final test for chip shipment before delivery to the customer. IQC test system includes QA test and QC test.

10.2.1. QA Test

QA test is a testing for each function module of chip based on Android system, which can judge whether chip can reach production standard by system total running results, single module testing fluency.

10.2.2. QC Test

QC test is used to test each module code booting from Nand flash, and run schedule by using PC control code, then read the return value of each module testing. If the return value is PASS, then continue to perform the next module testing; or else stop testing and remind the testing module FAIL.

11. Part Marking

Figure 11-1 shows the H616 marking.

Figure 11-1. H616 Marking

Table 11-1 describes the H616 marking definitions.

Table 11- 1. H616 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	H616	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

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Contact US:

Service@allwinnertech.com

www.allwinnertech.com